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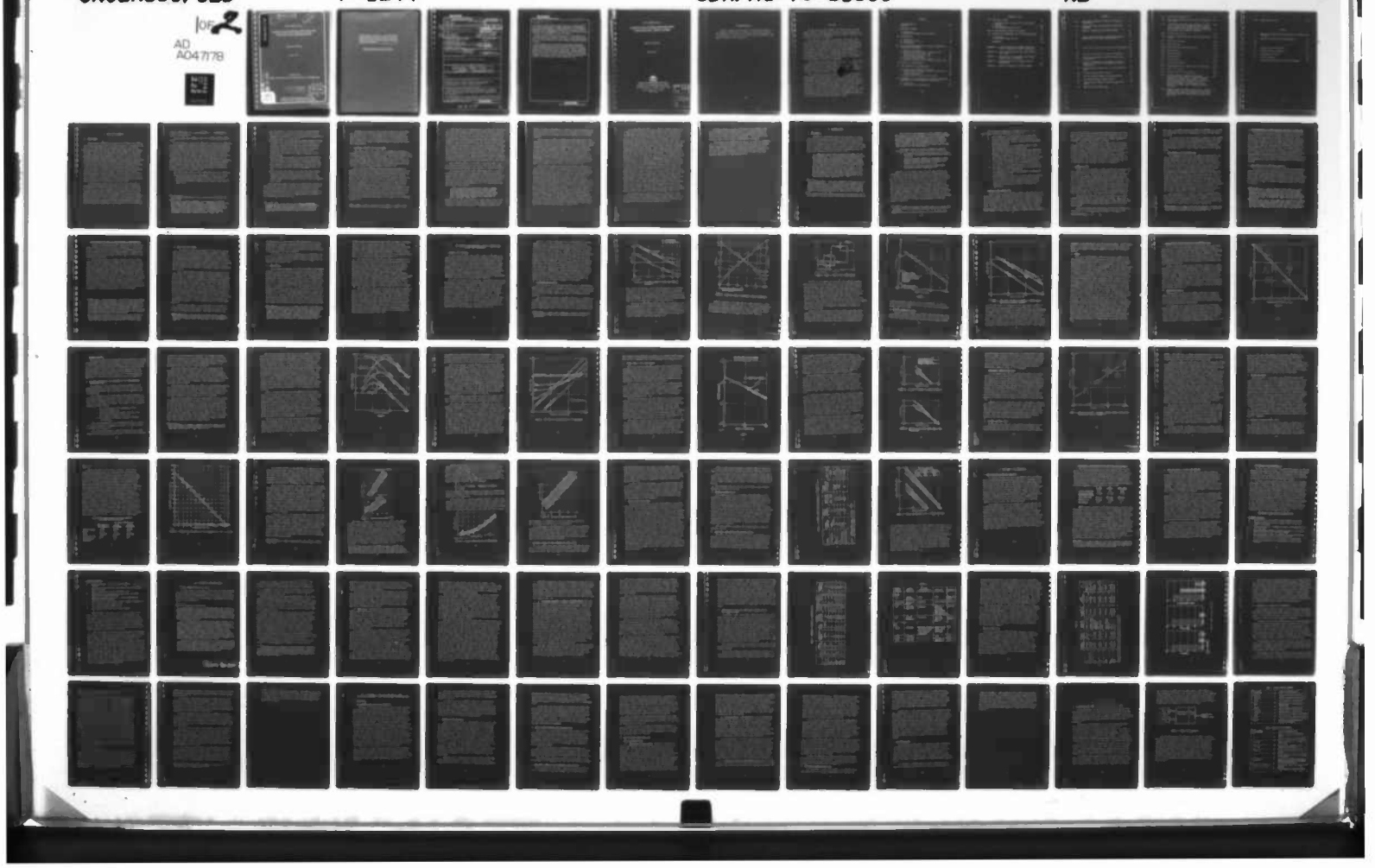

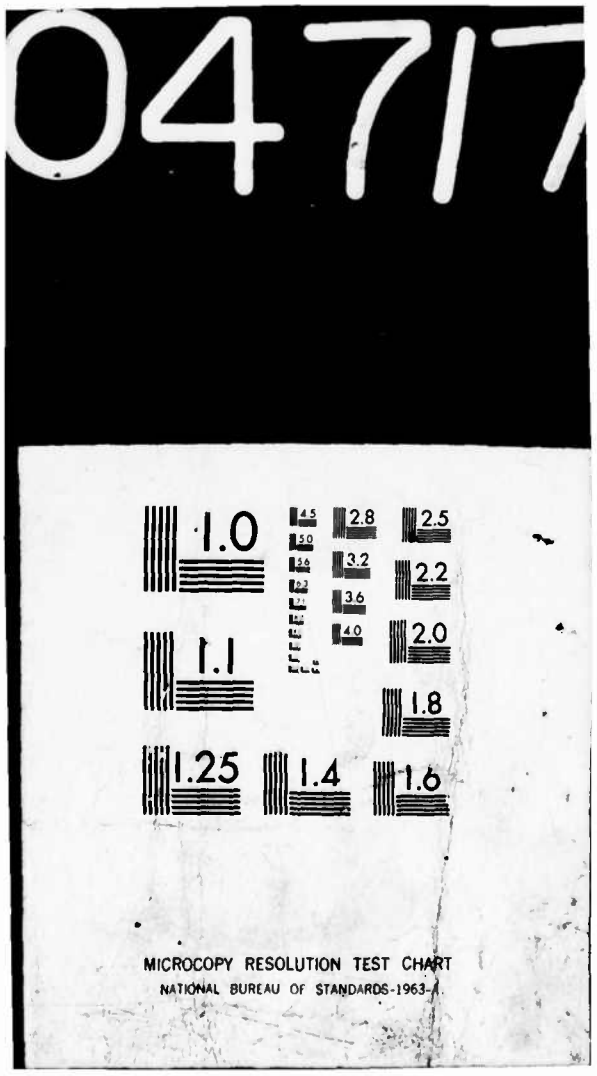
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LARGE SCALE INTEGRATED CIRCUITS FOR MILITARY APPLICATIONS

Glenn W. Preston

May 1977

Prepared for

Office of the Director of Defense Research & Engineering

INSTITUTE FOR DEFENSE ANALYSES
SCIENCE AND TECHNOLOGY DIVISION

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(U) Two categories of cost are analyzed: the direct life cycle cost of the integrated circuit assemblies (development, acquisition, spares

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(U) The economic and physical characteristics of several types of integrated circuits are reviewed, particularly as they depend on the level of circuit integrations, and the effect of these characteristics on the total life cycle cost of several classes of military systems is examined.

(U) The potential for cost avoidance or performance improvement through the application of current integrated circuit technology to military systems is estimated as several billion dollars for weapons systems and intelligence gathering systems which are now in advanced development or in the early stage of production. Various steps that might be taken by DoD to partially achieve these cost reductions are discussed, the chief one being a study of the feasibility of designing a family of integrated circuits which could replace a significant fraction of the circuits which would otherwise be used.

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Glenn W. Preston

May 1977

INSTITUTE FOR DEFENSE ANALYSES
SCIENCE AND TECHNOLOGY DIVISION
400 Army-Navy Drive, Arlington, Virginia 22202

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ABSTRACT

The gap which exists between the current state of integrated circuit technology and its use in military systems is broadly discussed and analyzed, and the economic incentive for narrowing this gap is examined.

Two categories of cost are analyzed: the direct life cycle cost of the integrated circuit assemblies (development, acquisition, spares and repairs), and the systems support life cycle costs (the marginal cost of the military weapons system attributable to carrying and supporting these assemblies, including prime power, air conditioning, desk space, loss of operational readiness due to integrated circuit failures, etc.). The dependence of these costs on the physical characteristics of the integrated circuits is discussed.

The economic and physical characteristics of several types of integrated circuits are reviewed, particularly as they depend on the level of circuit integrations, and the effect of these characteristics on the total life cycle cost of several classes of military systems is examined.

The potential for cost avoidance or performance improvement through the application of current integrated circuit technology to military systems is estimated as several billion dollars for weapons systems and intelligence gathering systems which are now in advanced development or in the early stage of production. Various steps that might be taken by DoD to partially achieve these cost reductions are discussed, the chief one being a study of the feasibility of designing a family of integrated circuits which could replace a significant fraction of the circuits which would otherwise be used.

CONTENTS

CONTENTS (Cont.)

FIGURES

TABLES

I. EXECUTIVE SUMMARY

A. BACKGROUND

This report presents the results of a study by the Institute for Defense Analyses (IDA) of recent advances in integrated circuit (IC) technology and the possible effects on the costs and capabilities of military intelligence gathering and weapons systems. The study was conducted at the request of the Deputy Director (Policy and Planning) in the Office of the Director, Defense Research and Engineering. Owing to the high level of activity and rapid rate of advances in IC technology, information for this study was developed largely through direct personal contacts within the semiconductor industry, university laboratories, military contractors, government-supported nonprofit research centers, government laboratories, military procurement groups and their technical support organizations, Defense Advanced Research Projects Agency, and the Office of the Secretary of Defense. The program involved 18 man-months of effort, approximately 6 man-months of which were provided by consultants and the remaining 12 man-months by the IDA staff.

The principal topics dealt with include the costs of IC development and production; the effect of circuit integration on the cost of the host system; the current state of IC technology; IC performance requirements for military systems; and certain relevant institutional, managerial and policy issues. These results indicate that substantial economic and performance incentives exist for the utilization of more advanced IC technology in military systems and that the impediments to realizing the potential advantages in performance and cost (presented

by this technology) are chiefly institutional and managerial rather than technical.

The picture that emerges is one of a rather complex situation.

The IC industry itself was created in large part by vigorous, young, imaginative scientists (in many cases also entrepreneurs) and its spectacular growth was propelled by breathtaking advances in productivity based on new semiconductor device and production technology. This has created a remarkable demand for various types of ICs. The IC industry seems impatient with military procurement practices, which are often slow, piecemeal,* and encumbered with elaborate documentation and qualification procedures. Their greatest profits have come from the high-volume consumer and industrial markets which require only modest performance; whereas, the military applications demand much in performance but offer little in IC production.**

On the military side, we find (from this and other studies):

- escalating performance requirements for military intelligence gathering and weapons systems, which lead to increasing equipment complexity and overall unreliability (Ref. 10);

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* Consolidated procurement of ICs is practiced in the NSA but not in DoD.

** According to a recent editorial, which appears to reflect the view of many IC manufacturers, "...Military specifications and buying practices are antiquated and burdened with red tape...(DoD) is unable to keep pace with semiconductor technology. LSI devices...are...forced by unreasonable processing, inspection, and test standards to be prohibitively expensive...electronics firms who do...business with the government earn lower...pretax profits." (Ref. 57)

- the expenditures of tens of billions of dollars/year which are not subjected to critical analysis by the managerial techniques of cost accounting or productivity analysis (Refs. 1, 14 and 24);*
- procedures for developing and procuring weapons systems in which full-scale production is often preceded by a long and (comparatively) meagerly funded engineering development program (Ref. 28); typically, equipment design and parts lists are frozen years before deployment, effectively precluding subsequent custom LSI updating;
- out-year operations support problems involving complex test equipment, a proliferation of special components and the necessity of replacing failed components which are sometimes no longer commercially produced (in some cases decades after the initial deployment) (Ref. 2), and
- that military applications, for the most part, require higher performance (speed) than the commercial and industrial applications which absorb the bulk of the present large scale integrated circuit (LSIC) production (see below).

Thus, although there is much to be gained from the use of advanced LSICs in military systems, the commercially developed circuits are mostly useful only at the low-speed end of the military demand spectrum, and the military project managers and systems project offices share an understandable reluctance to use higher speed custom circuits.

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*A recent issue (April 1977) of the Defense Management Journal discusses the application of productivity analysis in DoD. To apply these concepts to military operations would require the establishment of cost accounting and capability audit procedures--an ambitious undertaking.

Although the purposes of the present study were fact-finding and analytical, and the examination of possible remedial measures was left to a future study, much of the material presented here points to the desirability of a joint service program to develop a family of high-performance circuits for military applications.

B. PRINCIPAL FINDINGS AND CONCLUSIONS

The direct life cycle costs for IC assemblies in military equipments currently is estimated to exceed $400 million/year and to be growing at about 20 percent/year*. The systems support costs, i.e., the marginal cost of the host system for prime power, air conditioning, deck space, airframe weight, fuel, etc., attributable to IC assemblies, often equal and sometimes greatly exceed the direct costs of these assemblies (Section III).

Most dedicated military digital processing equipment in weapons systems and intelligence gathering systems which are now deployed, in production or engineering development, contain the 54/74 TTL small and medium scale integrated circuits (SSICs, MSICs) whose physical characteristics (size, weight, reliability and power consumption) per function are inferior--by about an order of magnitude--to circuits which embody the best current bipolar technology; moreover, their production cost/gate is correspondingly higher. Further, military program managers and systems project offices are often motivated to continue the use of the 54/74 series TTL MSICs rather than either commercial or custom LSICs, notwithstanding the potential life cycle cost savings and performance improvements, for reasons to be presented (Section IV).

*This figure includes operational and logistics support costs.

Some reasons for the widespread use of the 54/74 series are that they have adequate speed for most applications, they are qualified for most military environments, are in widespread use, are available from multiple sources--and have become de facto standards which represent no recognized risk to program cost, schedule, or out-year availability. On the other hand, special (custom) LSICs are expensive to qualify, difficult to second-source and are perceived to involve risks with respect to schedule, nonrecurring costs of development and documentation, and availability for out-year logistics support. The latter reservation applies also to the newer commercial bipolar LSICs (bit slices, microprocessors). Individual weapons systems programs infrequently require a sufficient quantity of LSICs to justify--on the basis of procurement cost--the development of new circuits.

The continued heavy use of MSICs is possibly due, in part, to an incomplete recognition of the total life cycle cost (particularly the systems support costs) impact of circuit integration.

An examination of the steps which might lead to a better utilization of advanced IC technology in military equipment reveals issues which are managerial and institutional in nature rather than technical; issues having to do with the division of responsibility for procurement and out-year operational and logistics support, standardization, etc. To quote an earlier NSA study of this subject:

> ...LSI can provide vast reduction in size, weight, cost and power requirement of electronic systems... [yet] despite early recognition of its potential, and heavy funding of its development, DoD has made little progress implementing LSI in military systems...the barriers...[being] more bureaucratic than technical. [Ref. 24]

However, there are other barriers to LSIC usage in DoD. For example, IC manufacturers find their biggest markets in the commercial sector, and because of dissimilar military and

commercial LSIC requirements in respect to both performance and physical characteristics, they do not emphasize the development and production of the types of ICs most suitable for military systems.

Nevertheless, several commercially developed medium- and high-speed LSICs have been introduced and are beginning to appear in military systems, and this process, if left to itself, might eventually lead to de facto standardization on a new family of more highly integrated circuits. Also, advanced ICs specifically intended for military systems are currently being developed at (1) dedicated semiconductor facilities which are adjuncts of weapons systems facilities (such as Raytheon and Westinghouse), (2) a few IC manufacturing divisions of corporations with substantial interest in military business (such as TRW, TI and Hughes), and (3) MIT Lincoln Laboratories.

Military intelligence gathering and weapons systems have, over the past 35 years or so, grown steadily more expensive, complex and unreliable, while at the same time their components generally have been improved in reliability, performance and--in the case of microelectronics--in price. This trend in systems cost and reliability is directly correlated with progressively higher systems capabilities and is traceable not to technological developments or institutional workings so much as to national defense policy--specifically, to the criteria by which we design our fighting equipment. If military systems are designed to specified cost or performance goals, then a better utilization of IC technology would give significant performance improvements in the first instance or cost avoidance in the latter. But, if every advance in the technology of ICs (or other components) is seized upon to justify higher performance goals, then the trend toward more expensive, complex and unreliable systems would continue. (See p. 44.)

Our study indicates that if a relatively small number (500 or fewer) of ICs with a few hundred gates each, using medium- to high-speed technologies (such as LS TTL, I^2L, mixtures of I^2L and TTL, 3D, silicon gate CMOS) could be identified with which a substantial part of military IC equipment could be fabricated, then substantial economies in direct life cycle costs and systems support costs could be effected, and the estimated level of demand for these circuits would be adequate to support production at economic levels. And, logistics costs could be minimized by avoiding the unproductive proliferation of device types and their associated test equipments. The possibility of defining a small but versatile set of military standard circuits depends first on the degree of commonality among the various requirements for IC assemblies in military systems, and second, on the possibility of partitioning logical networks into groups of LSICs (with at least a few hundred gates each) within the constraints imposed by packaging (particularly the number of available pins) (Section VIII). The cost of developing such a family would be least if gate-array circuits were used. LSI gate-array circuits have been developed in medium- and high-speed technologies (10 MHz, 40 MHz) from which logical designs can be implemented by designing and applying a final metallization layer to the chip. Using computer-aided design (CAD) software, new 300-gate circuits are now being designed, developed and tested at a reported average cost of $10K, and in six to eight weeks' elapsed time. Gate utilization averages about 80 percent, which compares well with 54/74 MSIC assemblies (Section V).

The utilization of LSICs in military systems would also be facilitated by the standardization of mask formats, test and design information, which would simplify design transfers and second-sourcing of new circuit designs (Ref. 58).

Military weapons systems could benefit more readily from future advances in microelectronics if IC assemblies were designed in the future to facilitate plug-compatible retrofits with circuits of more advanced technology. This should be an integral part of any circuit standardization program.

This might be accomplished by using a hierarchical organization of IC modules and higher level assemblies (such as hybrids). Those weapons systems now in engineering development or production that contain large IC assemblies should be examined for the life cycle cost advantage of retrofitting with plug-compatible assemblies of more advanced ICs.

II. INTRODUCTION

A. BACKGROUND

During the last dozen years or so, advances in microelectronic technology have improved the physical and performance characteristics of ICs and lowered their production costs to a degree that can only be described as revolutionary. The IC is smaller, lighter, more reliable, consumes less power and is cheaper to produce--by orders of magnitude--than an equivalent assembly of discrete circuits.*

> The cost reductions resulting from higher levels of integration (i.e., more circuitry on each chip) have been remarkable. The individual diffused transistor sold for a price of approximately one dollar in 1961, a few years after its introduction. Today, a (commercial grade) 1024 bit memory containing over 6000 transistors also sells for about one dollar...representing a cost reduction of about 6000:1 in 15 years. The resulting effect on equipment costs can be seen in the electronic calculator, which has been reduced in cost by a factor of 500:1 in the last 8 years.** Also, as circuit complexity has increased, the reliability of the individual circuit has remained approximately constant resulting in a proportionate improvement of reliability per gate. [See Fig. 7, p. 36]

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*The benefits of the IC are also remarkably unmitigated by adverse consequences: no scarce resource is consumed; integrated circuit production requires relatively little power, creates little pollution, and involves minor capital investment in relation to its contribution to the gross national product. For a discussion of the impact of microprocessor-controlled automobile ignition on fuel economy, see Ref. 30

**The conversion to real relative prices by the application of the general inflation factor would nearly double these ratios.

This increase in integrated circuit complexity has also resulted in a cost savings in the subsequent assembly into digital processing hardware, as well, since more of the total interconnections are made within the semiconductor components, which have proven to be more reliable than those at the next higher level, resulting in an increase in overall systems reliability. The costs of cabinets and cables and total power and cooling requirements all have been reduced.

The higher levels of circuit integration (which have made all of this possible) have been achieved by:

1. Decreasing [the] minimum dimensions [of circuit elements] resulting in higher density of circuit elements;
2. Decreasing defect density in the silicon wafer through improved processing techniques, allowing the practical production of circuits of larger area [Ref. 28, p. 242], and
3. Innovation in circuit forms allowing higher functional density. [Reference 6.]

However, at the present time, in most applications the integration of military digital circuits has progressed only to the medium scale integration (MSI) level, about 20-60 gates* per chip (using circuit technology five to ten years old), compared to 4000 gates per chip in circuits developed over the last five years and widely used in consumer and commercial applications.** The chief purposes of this study are to estimate the performance and economic incentives for introducing more highly integrated circuits in military systems, to analyze the deterrents to their introduction, and to suggest DoD initiatives that might minimize, if not eliminate, these deterrents so that the potential economic and performance advantages might be realized.

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*A "gate" embodies an elementary logical function such as AND, OR, NAND, etc., and typically includes five to ten active elements.

**These include the microprocessors, such as the INTEL 8080.

As this study progressed, it became clear that diverse and complex issues are involved, relating to:

1. the economics of IC development and production;
2. the performance requirements of IC assemblies in military equipment, weapons systems and intelligence gathering systems;
3. the characteristics of the various types of ICs, particularly speed and integrability;
4. the "out-year problems" of maintenance and logistics support for systems with operational lives covering 20 years or more using IC technology with an economic life span of five years or less (in some cases);
5. the various incremental costs to the host system of carrying and supporting IC assemblies and how they relate to the characteristics of the circuits;
6. the degree of commonality among the IC requirements of various military equipments;
7. the comparative benefits and penalties of mandatory standardization, and
8. the institutional factors--the roles and motivations of the various corporate and bureaucratic groups which participate in the design, development and operations of military equipment containing IC assemblies.

1. Potential Cost Reductions

With respect to the possible economic incentives for introducing more highly integrated circuits into military systems, in 1975 the purchases of IC devices by the U.S. military totalled nearly $300 million* (estimated), and at the current estimated rate of growth (20 percent/year), the direct outlay for equipment consisting principally of ICs would total about several billion dollars over the next decade at present price levels.

*This figure includes boards, cabinets, secondary power supplies.

(It has been estimated by qualified Naval personnel that the BQQ-5 and BQQ-6 systems alone, when fully deployed, will contain nearly one billion dollars worth of digital processing equipment consisting principally of ICs.)

In addition, the marginal life cycle costs of the host systems indirectly attributable to IC devices (such as power supplies, air conditioning, air frame weight, fuel) appear to be about equal to the direct acquisition and maintenance costs for a total figure of $10 to $20 billion. (See Sec. III, below.) Therefore, the total foreseeable military expenditures over the next 10 years or so, which are related directly or indirectly to IC devices, justifies a considerable effort to realize the full benefits of circuit integration.

2. Classes of ICs

There are two principal classes of mature IC technologies*; the bipolar and the field effect (generally a metal oxide semiconductor--MOS). The bipolar class of circuits are faster by one to two orders of magnitude, but are usually produced with less than a few hundred gates/chip (with the exception of the so-called integrated injection logic--I^2L--circuits). They are, as a group, more difficult to manufacture (although this fact is somewhat obscured by the enormous experience in these technologies), and hence more expensive. The principal bipolar technologies in the order of their increasing speed are I^2L, TTL, LS TTL, ECL. (See Terminology, Section C, below.)

Field-effect MOS circuits can be produced with several thousand gates/chip at a startlingly low price. There are three principal types of MOS technologies: PMOS, NMOS and CMOS (which combines PMOS and NMOS transistors to obtain certain advantages).

Both the bipolar and field-effect devices will make major contributions to military weapons systems technology, but

*See Terminology, p. 17.

they are by no means equivalent because the maximum clock speed of current MOS circuits is inadequate for many military applications.*

For the most part, MOS technology is applied at the higher levels of integration (a few thousand gates/circuit); MOS does not, or cannot, compete with the faster, more flexible, more varied bipolar circuits at the lower levels of integration, notwithstanding the fact that bipolar is generally more expensive.

3. The Economics of IC Production

The aggregate cost of ICs is commonly allocated to: the nonrecurring costs of prototype development, which include design engineering, mask preparation, design verification, testing, etc.; start-up costs, which consist of the costs of establishing manufacturing process control and marginal production cost, which is the manufacturing cost/circuit when the rate of production has reached an economical level. In contrast to the marginal (or unit) cost of ICs at high and sustained rates of production, the nonrecurring costs associated with designing, testing, and tooling for a new circuit design sometimes reach one million dollars (depending on the level of integration, circuit technology, etc.) and cannot be justified unless many thousands of circuits are needed; whereas, under present procurement policies, military purchases of specialized custom highly integrated circuits would often involve only a few hundred IC devices of any given type.

The development of a family of LSICs, standardized for military applications, is economically attractive only to the degree that the nonrecurring costs, in addition to the costs of documentation, qualification, etc., can be distributed over a sufficiently large number of military equipments.

*This situation may change with the introduction of faster MOS technology (such as DMOS) or by the development of circuitry which substitutes parallelism for speed (Ref. 33).

4. The Constraint on Circuit Design Imposed by Integration

Although an arbitrary collection of logical circuitry can be mounted on a chip, the number of pins and tabs is limited by the dimensions of the chip to about 60. Thus, a collection of digital circuits cannot be divided arbitrarily into blocks containing a few thousand gates, each designed into a chip. Rather, blocks must be identified that can be linked together by 60 or fewer lines.* At higher levels of integration, the delineation of circuitry to be integrated onto a single chip is a difficult, innovative process--not a straightforward engineering exercise--particularly if the circuit is to be of sufficient flexibility and generality that its aggregate uses will sustain its production at economical levels.

5. Characteristics of Military Circuits

Most military uses of digital circuitry such as general purpose computers; sonar beam forming and spectral analysis; radar signal processing; speech abstraction, coding and synthesis, and message encoding and decoding, require clock speeds which exceed the capabilities of current MOS technology** but are within the range of bipolar technologies (Ref. 32, Section IV, below).

*The serial shift register satisfies this condition almost trivially since it requires pins only for the input and output bytes, power and clock, ground, and a few control signals. The random access memory device becomes possible at a higher level of integration where there are sufficient gates on the chip to include the address decoding network, and so on.

**Currently, the bulk of LSIC production consists of microprocessors, memory chips, programmed logic arrays, etc., which are used in applications such as hand calculators, wrist watches, TV games, industrial process control, controllers for consoles, displays, tape drivers, etc.; and, in all of

6. Corporate Motivations and Intercorporate Relationships

Several corporate groups must contribute to the development, production, installation and maintenance of customized LSICs for the military, including the IC manufacturer, the weapons systems supplier, the program manager or systems project office for the procuring services, and the Office of the Secretary of Defense.

IC manufacturers, as a group, probably lack the knowledge of military systems requirements that is needed to define a family of standardized military LSICs (the more highly integrated circuits are necessarily more specialized and must meet more boundary conditions imposed by the system in which they are embedded); while the major weapons systems suppliers often do not have highly qualified IC design teams. Both are motivated to maximize their gross sales.* The military weapons systems program manager usually lacks the resources to develop either custom ICs or specialized digital processing devices. For these reasons, initiatives may be required at the DoD (the Office of the Secretary of Defense) level if LSIC developments responsive to DoD requirements are to be forthcoming.

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these cases, the clock speeds of the MOS devices are adequate. if not ample. These same types of ICs will also find widespread applications in military systems. Higher speed is a byproduct of further miniaturization and integration, and this trend may eventually lead to faster MOS. Nonetheless, in most military applications requiring large numbers of ICs, MOS devices are not used, possibly due to the reluctance of design engineers to resort to multiplexing and parallelism (to achieve the required processing speed).

*IC manufacturers attempt to do this by entering the end product business (wrist watches, hand calculators, TV games, minicomputers), while the weapons systems suppliers sometimes develop proprietary IC devices for the same purpose.

B. OBJECTIVES AND SCOPE

The present study was chartered to review the current state of LSIC technology and production economics, examine the benefits of and deterrents to the use of custom LSICs in military systems, investigate the potential for reducing IC lead time and nonrecurring costs, compare the various circuit technologies and assess their possible contribution to military systems design, and investigate the implications of custom LSIC utilization with respect to electronic module standardization, etc.*

This paper extends the scope of earlier studies in several ways. It includes an analysis of the approximate total direct cost of ownership of digital IC devices (as they relate to the level of circuit integration), including the nonrecurring development cost, production or unit costs, maintenance and spares; also the systems support cost, i.e., the marginal cost of the weapons system itself allocatable to carrying and supporting the IC device. The economic analyses are based on empirical and theoretical relationships for the physical and economic properties of ICs relative to the level of integration used, in conjunction with a simple life cycle cost analysis to estimate the total economic incentives for developing a standardized family of ICs at various levels of circuit integration.

Almost every aspect of IC technology is in a state of rapid evolution and there exists a variety of circuit techniques and production processes. The various forms of IC

*LSIC technology is the subject of several earlier studies sponsored by the Air Force (Refs. 22, 23, 27), the National Academy of Sciences (Ref. 25), NSA (Ref. 24), and NAVAIR (Ref. 2).

devices differ in cost, speed, power dissipation, level of integration, operating temperature range, and so on, which affect their suitability for custom military applications. Therefore, a summary of the characteristics of the established IC technologies has been included.*

The deterrents to the introduction of custom LSICs (as seen by the weapons systems program manager or systems project office) have been dealt with in earlier studies but are reviewed and restated here.

C. TERMINOLOGY

Where special meanings of words are implied, this report attempts to use them in their generally accepted sense. The term "integrated circuit" here refers to the circuit elements mounted and interconnected on a single chip. "Semiconductor technology" refers to the physical aspects of IC fabrication (diffusion, ion implantation, epitaxial growth, etching, plating, etc.). "Circuit technology" refers to the actual structure or arrangement of "P"- or "N"-type regions, junctions, insulating regions, contacts, etc., to produce useful circuit elements as, for example, merged transistors (for current injection, as in I^2L), current-switching bistable elements (as in ECL), etc. "Bipolar technology" refers to the collective semiconductor technology used to produce bipolar ICs, as distinct from field-effect or MOS circuits. The Schottky clamp (or diode) involves distinctive fabrication and also provides

*The continued presence in the market of such a diversity of IC types shows that there is no one solution for all applications; the three common forms of MOS and the three or four common forms of bipolar are not strictly comparable with respect to yield, throughput capacity, power consumption, and level of integrations, although I^2L has performance characteristics to dominate and eventually replace the MOS devices except in the low-price, low-performance market.

unique circuit characteristics and might, therefore, be referred to as both a semiconductor and a circuit technology. "Module," specifically refers here to a collection of ICs and possibly other components, interconnected and mounted on a board, as in a Standard Electronics Module. "Device" refers here to the functional type of circuit such as arithmetic logic unit, shift registers, random access memory, etc.

The term "custom" indicates ICs that are designed for a special purpose or application and are not intended to be produced on a regular basis for general use. In this report, acronyms have been avoided except with reference to semiconductor and device technologies: I^2L refers to integrated-injection logic, ECL to emitter-coupled logic, TTL to transistor-transistor logic, NMOS to "N" (negative charge) carrier metal oxide semiconductor, PMOS to "P" (positive charge) carrier MOS, CMOS to complimentary MOS (both NMOS and PMOS in the same gate), LS TTL to low-power Schottky TTL, SFL to substrate fed logic, DMOS to double diffused MOS, etc.; 3D signifies a triple diffusion bipolar process practiced by TRW.

The term "life cycle cost," here refers to the cumulative costs of a system or equipment, including development, production, installation, maintenance, logistics, training manuals, special test equipment, and so forth. The term "direct life cycle cost" refers to those costs directly associated with a piece of equipment, whereas "system support life cycle costs" refers to the marginal life cycle cost of a weapons system attributable to carrying and supporting a piece of equipment. This would include the marginal costs of the weapons system associated with the prime power supply, air conditioning, air frame weight, deck space, fuel, etc.

III. THE ECONOMIC IMPLICATIONS OF CIRCUIT INTEGRATION IN MILITARY EQUIPMENT

A. GENERAL COST FACTORS

In this section, life cycle costs (LCCs) of military systems which contain digital electronic equipment are discussed, based on the actual direct acquisition and development costs of IC assemblies, and on their physical characteristics (used in conjunction with cost coefficients to estimate the systems support costs). Both the direct costs and the physical characteristics depend strongly on the level of circuit integration. The purpose of this approximate analysis is to indicate the aggregate economic incentive for the introduction of more highly integrated circuits in military weapons systems.

The sources of LCCs considered are: production, nonrecurring development, maintenance (including spares), and systems support (both acquisition and maintenance). During this study, some data were compiled on production and nonrecurring development costs, but no specific information was sought or discovered pertaining to maintenance or systems support costs. Instead, an "order of magnitude" analysis of maintenance costs as they depend on circuit integration has been included. The details are found in Appendix A, which is similar in form and notation to standard cost models (Ref. 8). The treatment of maintenance costs consists principally of analyzing the implications of the reliability of ICs in logistic turnaround time, etc.

Some of the above components of LCCs are subject to future changes in input costs (material, labor), pricing policy, vertical product integration (which may result in the ICs not being offered except as part of a larger assembly), etc., none of which can be well foreseen. However, the systems support costs, which are relatively well defined, depend on the physical characteristics of the device itself, although the cost coefficients (which relate physical properties to cost) are also subject to future changes. However, our interest here focuses primarily on the relative costs at different levels of integration, and it is difficult to imagine underlying economic factors that might change future costs differentially in relation to the level of integration. Future developments in IC production technology might conceivably have such an effect, but all research efforts in this area are aimed in the direction of higher circuit integration, which would have the effect of strengthening the principal findings of this study.

1. IC Manufacturing Costs

The history of IC development has been one of progressively higher levels of circuit integration and lower selling price/gate, as portrayed in Figs. 1a and 1b. The former shows a stabilizing of the prices of SSICs, MSICs and LSICs at successively lower levels.*

The relationship between cost/gate and level of integration is shown in Fig. 2, where the currently quoted quantity price of seven representative military quality bipolar ICs from five different manufacturers are plotted. The solid line represents the price relationship used in the following life cycle calculations.

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* SSIC refers to small scale integrated circuits (10-20 gates/chip); MSIC to medium scale integrated circuits (20-100 gates/chip).

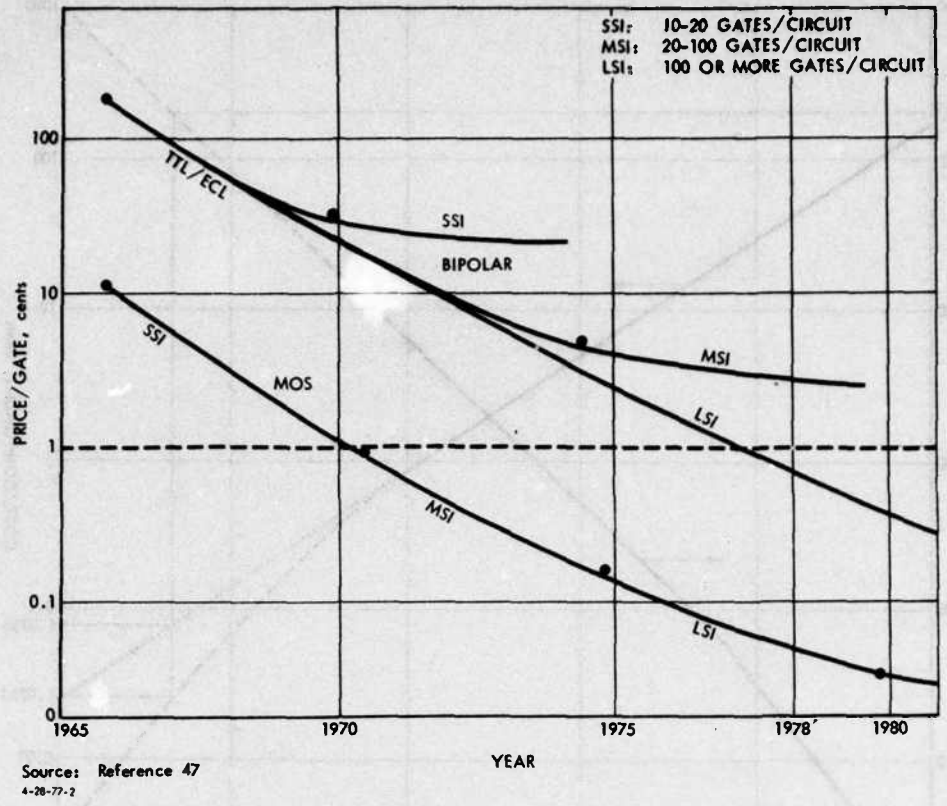


Figure 1a. Price/Gate (Commercial Grade) and Levels of Integration

The circuits shown here include microprocessors, a bit slice arithmetic processor unit, a 16-bit multiplier, a standard arithmetic unit and a 300-gate array. Memory circuits such as shift registers, read-only memories (ROMs), and random access memories (RAMs) tend to have relatively lower costs/gate, probably due to the regularity of their gate patterns.

The price relationship shown in Fig. 2 is similar to the corresponding one for commerical grade circuits obtained by replotting the data in Fig. 1c to show price/component vs. the level of integration (Fig. 3); the higher level of prices for the military quality circuits is attributable to the use of ceramic packages, additional testing, etc.

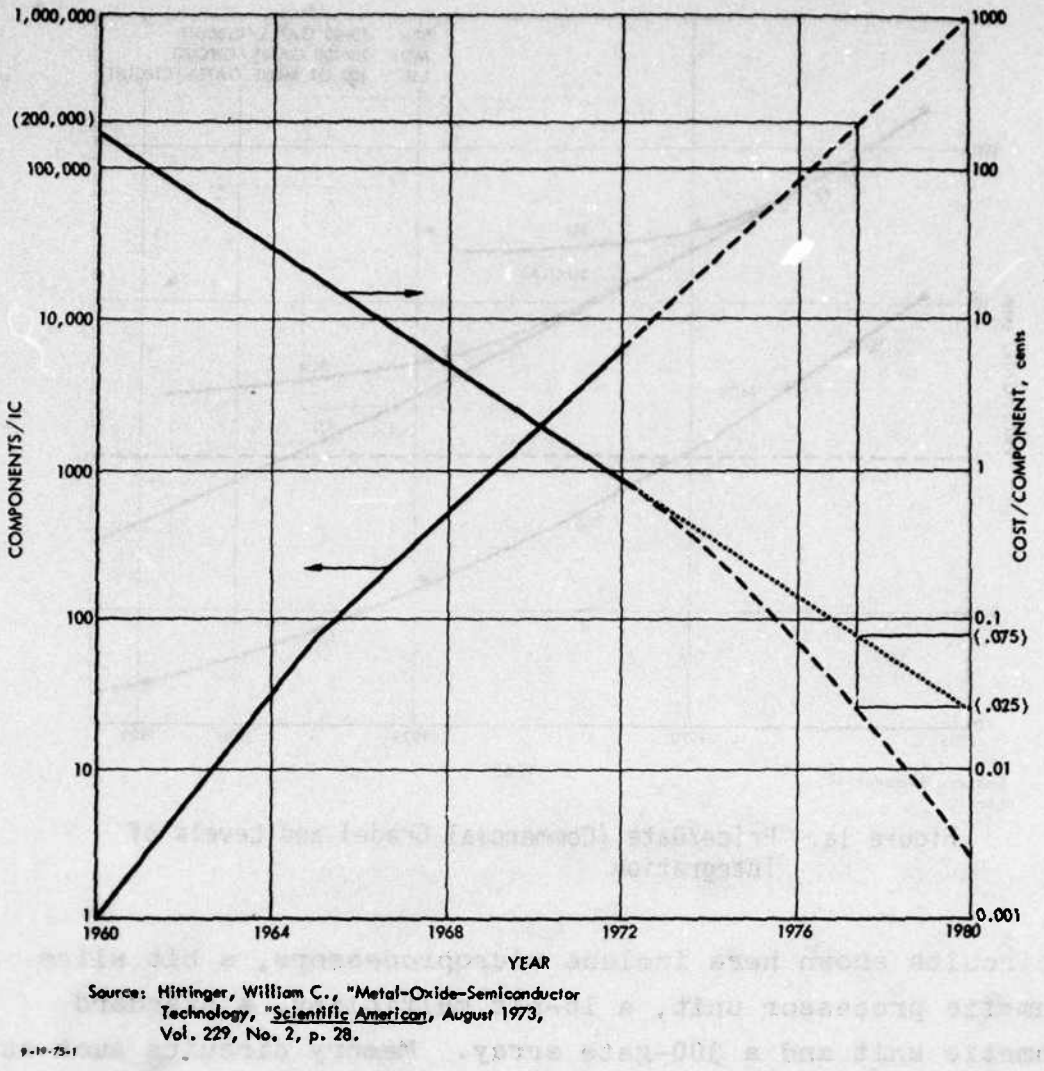
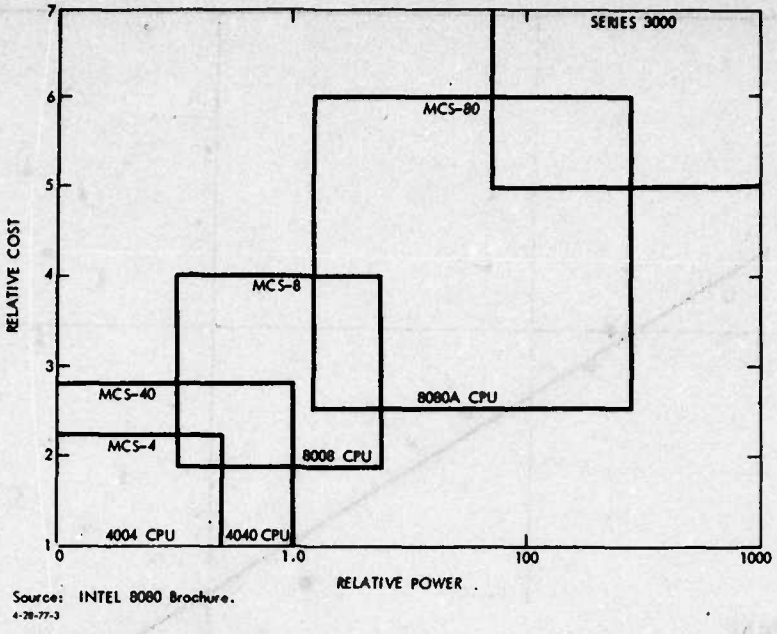


FIGURE 1b. Historical Trend of Components/IC and Cost/Component

INTEL's evaluation of computational power relative to cost for its own products is shown in Fig. 1c. Here the computational power/device increases approximately at the 3.5 power of price, which also corresponds to the slope of the price/gate vs. level of integration given by the solid line in Figs. 2 and 3.



Source: INTEL 8080 Brochure.
4-28-77-3

FIGURE 1c. Power vs. Relative Cost, INTEL Devices

In Fig. 3, the same price line has been plotted together with the price line for commerical ICs and other hypothetical price relations. The steeper dashed lines represent constant price/IC of $50, $100, and $300, while the upper dashed line depicts the cost/gate as varying inversely with the square root of the level of integration; at equal gate speeds, the corresponding computational power/circuit would increase as the square of price. This is sometimes known as Grosch's Law (Ref. 55, p. 41). The production cost of ICs in large quantities depends inversely on yield and directly on the size of the chip, as well as on the level of integration principally through its effect on chip size.

These price relationships reflect relative manufacturing costs at high rates of production (several thousand circuits/month). The demand for ICs customized to military requirements probably would not reach this level unless a standardized set of circuits could be developed from which a substantial part

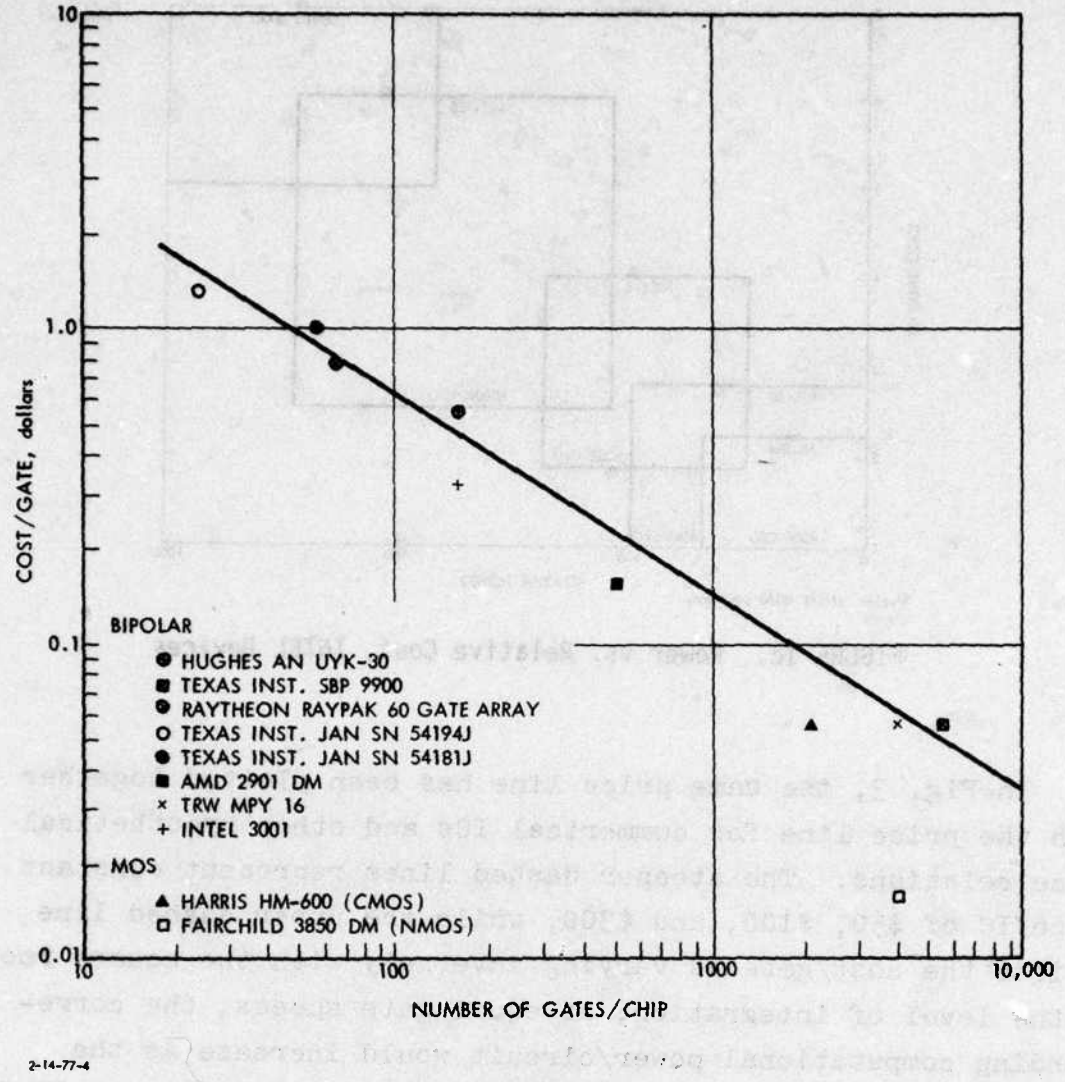


FIGURE 2.

of military digital systems could be fabricated. At low or erratic levels of demand, the unit cost could be substantially higher than that shown.

2. Boards, Connectors, etc.

Printed circuit boards, connectors, cabinets and power supplies also contribute to the direct life cycle cost of IC assemblies, but these add relatively little to the cost/gate except

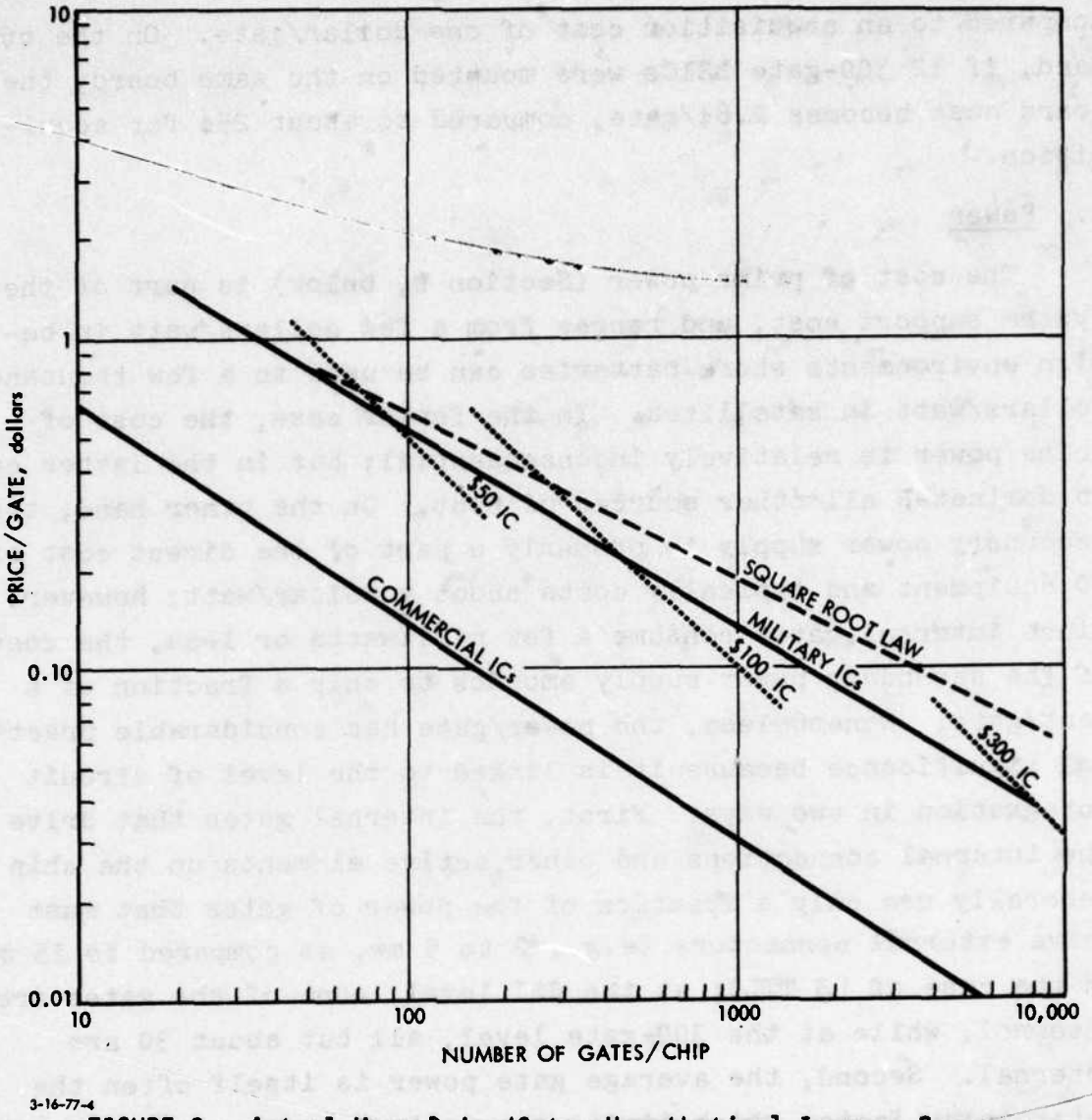


FIGURE 3. Actual Mean Price/Gate, Hypothetical Inverse Square Root Case, and Constant Price/IC

at very low levels of integration with small module cards or boards that have many layers of interconnections. In fact, their relative contribution to the gate cost actually diminishes at higher levels of integration since they tend to decrease in proportion to the level of integration, while the acquisition cost of the IC/gate diminishes more slowly, as we have just seen. For example, a 4" x 6" printed circuit board might mount 30 or more 20-pin dual-in-line packages containing, for instance, 600 gates, representing a cost of $.16/gate (for a $100 board),

compared to an acquisition cost of one dollar/gate. On the other hand, if 12 300-gate LSICs were mounted on the same board, the board cost becomes 2.8¢/gate, compared to about 25¢ for acquisition.

3. Power

The cost of prime power (Section D, below) is part of the system support cost, and ranges from a few dollars/watt in benign environments where batteries can be used to a few thousand dollars/watt in satellites. In the former case, the cost of prime power is relatively inconsequential; but in the latter case, it dominates all other sources of cost. On the other hand, the secondary power supply is properly a part of the direct cost of IC equipment and typically costs about a dollar/watt; however, since internal gates consume a few milliwatts or less, the cost of the secondary power supply amounts to only a fraction of a cent/gate. Nonetheless, the power/gate has considerable practical significance because it is linked to the level of circuit integration in two ways: First, the internal gates that drive the internal connections and other active elements on the chip generally use only a fraction of the power of gates that must drive external connectors (e.g., 2 to 5 mw, as compared to 15 mw in the case of LS TTL); at the SSI level, none of the gates are internal, while at the 300-gate level, all but about 30 are internal. Second, the average gate power is itself often the determining factor which limits the maximum level of integration because of the inability of the individual circuit to dissipate excessive heat. In other words, higher levels of circuit integration permit the use of lower power gates, and lower power gates permit higher levels of integration. The benefits of higher levels of circuit integration, therefore, have motivated the search for bipolar circuit technologies that have lower gate dissipation relative to speed (such as LS TTL, I^2L, and SFL).

4. Computational Power Relative to Acquisition Cost

To the extent that fast gates operating in serial are able to do the job of a proportionately greater number of slower gates acting in parallel, the computational capability associated with a circuit is proportional to its speed. Therefore, in addition to the unit cost/gate and average power, circuit speed (or inversely, the gate delay) must be taken into account in determining the relative costs of different IC technologies for any given application.

Figure 4 gives the gate delay (inverse of speed) vs. price/gate for the principal IC technologies. The diagonal line represents equal computational power/unit price. Points to the right represent lower computational power/unit price; points to the left are higher. Noteworthy in this figure is the superiority of ECL at 100 gates/chip to NMOS at 4000. This accounts, in part, for the extensive use of ECL (and other current-switching devices) in the largest commercial computers. It also indicates an economic incentive for the development of I^2L and 3D circuits for military applications.

5. Spares and Repairs

The comparative life cycle spares costs have a physical basis in relative reliability at different levels of integration, but the cost of labor for replacing a failed module or isolating and replacing a failed circuit has no precise meaning in a military operational environment.

The marginal cost of carrying and supporting electronic digital equipment in a weapons system also has physical bases--size, weight, power consumption and reliability of the circuit--and these are relatively well defined, particularly on a comparative basis. But the system's costs coefficients can only be based on estimates by qualified experts, an example of this being the value of a reduction in avionics weight (Refs. 4 and 20).

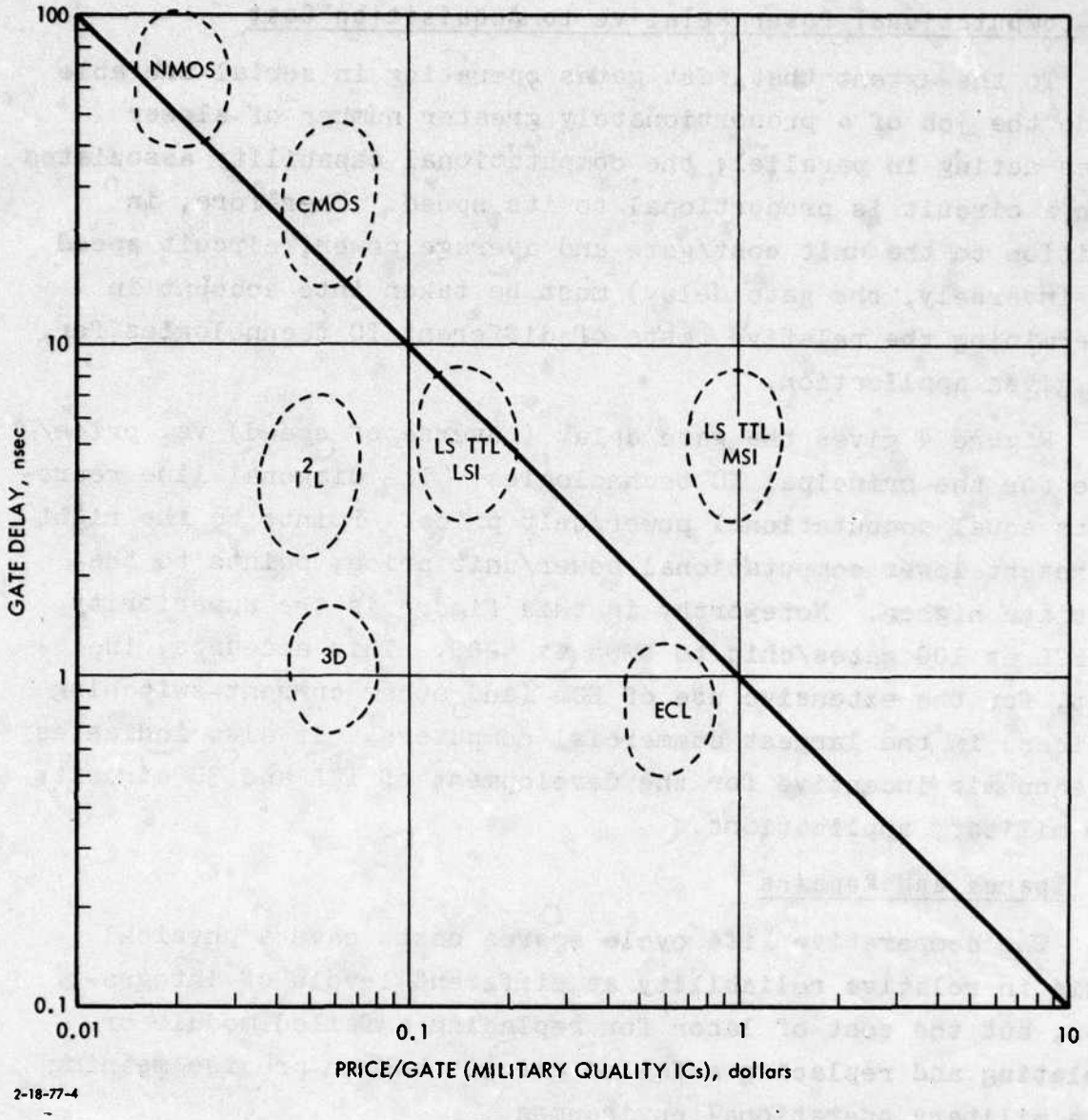

100
10
1
0.1
GATE DELAY, nsec
NMOS
CMOS
I^2L
3D
LS TTL
LSI
LS TTL
MSI
ECL
0.01
0.1
1
10
PRICE/GATE (MILITARY QUALITY ICs), dollars
2-18-77-4

FIGURE 4.

6. Systems Support

The systems support cost discussion presented below is based on approximate "back-of-the-envelope" calculations but is intended to show that a weapons system designed to carry LSIC assemblies can cost significantly less than one which must support equivalent assemblies of MSICs; indeed, in many applications, the systems support costs associated with IC assemblies are much greater than the direct life cycle costs of these assemblies, and also are more strongly dependent on circuit integration.

B. THE UNIT PRODUCTION COST COMPARED TO THE NONRECURRING DEVELOPMENT COST

An assembly of ICs provides a textbook example of the compromise between capital investment (in this case the nonrecurring development cost of the ICs) and the marginal cost of production.

The marginal cost of producing an additional assembly of ICs can be lowered if additional capital is supplied to develop more highly integrated circuits. But, at what level of production is the investment justified? The answer to this question depends on three things:

1. The IC production cost relative to the level of integration;
2. The nonrecurring development cost for a new, more highly integrated chip, and
3. The number of different circuits that must be developed.

The unit production cost of medium-speed bipolar circuits at various levels of integration is taken to be that given by the solid line in Fig. 2.

This formula is based on current prices, such as those shown, and on estimates received from responsible and knowledgeable

sources in the semiconductor industry. The prices at higher levels of integration could be somewhat lower than this if the rate of production were augmented by demand from the commercial sector, but the likelihood of this happening depends on the knowledge and skill of the circuit designer.

The nonrecurring development cost for a bipolar device starting with a logic design is taken to be $150/gate, independent of the level of integration; $600,000 for a 4000-gate chip; $45,000 for a 300-gate chip, and so on.* The development cost of a multilayer printed circuit board often reaches $20,000, but even at MSI level of integration, this usually amounts to less than about $10/gate.

When standard gate arrays are used, the nonrecurring development costs are much lower because only the design of the final metallization layer is involved. Raytheon reports typical total development cost of $10K for their 300-gate array LS TTL chip (or about $30/gate) and a design cycle of two months.

The actual development cost of a handcrafted circuit varies considerably, depending on the amount of rework (i.e., design or layout errors that need to be corrected), but average costs between $50/gate and $150/gate are generally assumed (Refs. 22, 23 and 28). The use of $150 in the present study is considered to be conservative since it lies at the upper end of the range quoted in the literature. If an entire family of 50 or so circuits were developed, some could be expected to incur abnormally high rework costs, but this would probably be offset by others that would require little or no rework costs.

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*"There appears to be general agreement that the nonrecurring cost will increase in direct proportion to the...density [of components on the chip]." (Ref. 49, p. C-7.)

The total nonrecurring cost for an entire family of circuits will also be proportional to the number of unique circuits from which the digital processing equipment is to be assembled. The worst case would be that in which the digital processing equipment contained only one IC of each type (shown by the dashed lines in Fig. 5). However, at lower levels of integration the circuits are simpler and fewer different types are needed, which is apparent from the limiting case of discrete components. The precise relationship between the number of unique IC types and the level of integration would not be the same for all systems (e.g., a system consisting largely of memory modules might need very few unique IC types), and a microprogrammable (variable architecture) bit slice family would probably need fewer members owing to its modularity with respect to word size and the more efficient gate utilization afforded by the architectural flexibility.

Figure 5 shows a well established empirical relationship (Refs. 28 and 30) for the number of unique circuit types for the central processor unit (excluding core memory) of a general purpose computer, in terms of the level of integration. Large commercial computer systems (2×10^5 gates), built of 100-gate ECL ICs, use about 100 different types of circuits, which indicates that the CPU incorporates the entire range of circuit types; in fact, experience indicates that 100 different circuit types are adequate at any level of integration and a much smaller number of carefully selected devices would fill the majority of gate functions in most systems (Refs. 53 and 54).

In the calculations of total nonrecurring development cost (below) a general relationship of the form shown in Fig. 5 is used for the number of unique circuit types, except that the maximum number is taken to be 100. Thus, in a system consisting of a total of 10^6 gates, if 100 types of 300-gate ICs were used, there would be about 30 of each type on the average and the

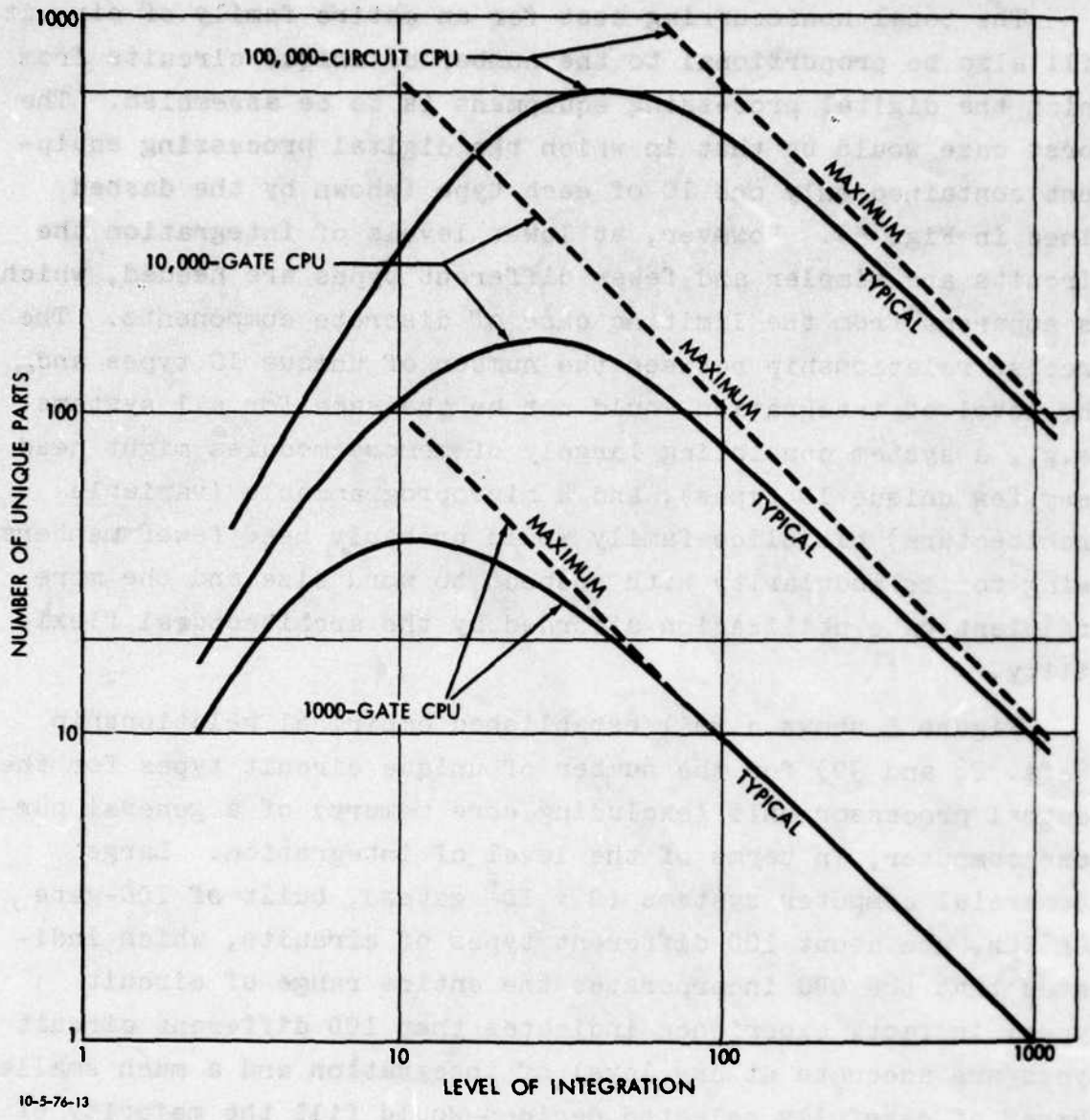
1000
100
10
1
NUMBER OF UNIQUE PARTS
100,000-CIRCUIT CPU
10,000-GATE CPU
1000-GATE CPU
MAXIMUM
TYPICAL
MAXIMUM
TYPICAL
MAXIMUM
TYPICAL
1
10
100
1000
LEVEL OF INTEGRATION
10-5-76-13

FIGURE 5.

estimated total nonrecurring circuit development cost would be $4.5M, assuming handcrafted circuits throughout. If a standard 300-gate array were used, the development cost would fall to one million dollars on the basis of the Raytheon experience.

This "part number" problem looms as a potentially serious limitation to integration levels. If the family of parts contains too many members, the demand for each type would be small and the price would exceed the assumed price formula (if the circuits were produced at all); whereas, if the family has too few members, the efficiency of gate utilization would generally drop. A common sense approach would be to develop circuits at the most economical level of integration in a technology compatible with the standard 54/74 TTL MSICs, developing the most frequently required circuits first, and filling out the system with standard MSICs. Circuits for general purpose computers might well be given first priority because of the potential for production support from the commercial market.

Combining these relationships for unit cost, parts count, and nonrecurring development cost, we derive the family of IC cost curves for systems containing 10^6 gates shown in Fig. 6.

The dashed lines show the unit acquisition cost (no nonrecurring development) for a family of 50-gate ICs and one of 500-gate circuits. The cost of an assembly of 500-gate circuits, excluding the IC development costs, would be just one-third of that for an assembly of 50-gate (standard TTL) MSICs if the 500-gate circuits replaced all of the 50-gate circuits without loss of gate efficiency. This figure illustrates another important economic effect, namely, that the existence of an already developed family of circuits suppresses the economic incentive to develop a new family of more highly integrated circuits. The development of a 500-gate/circuit family as an alternative to the standard MSI TTL family (about 50 gates/chip) would be justified by a procurement of about 30 systems, but if a 200-

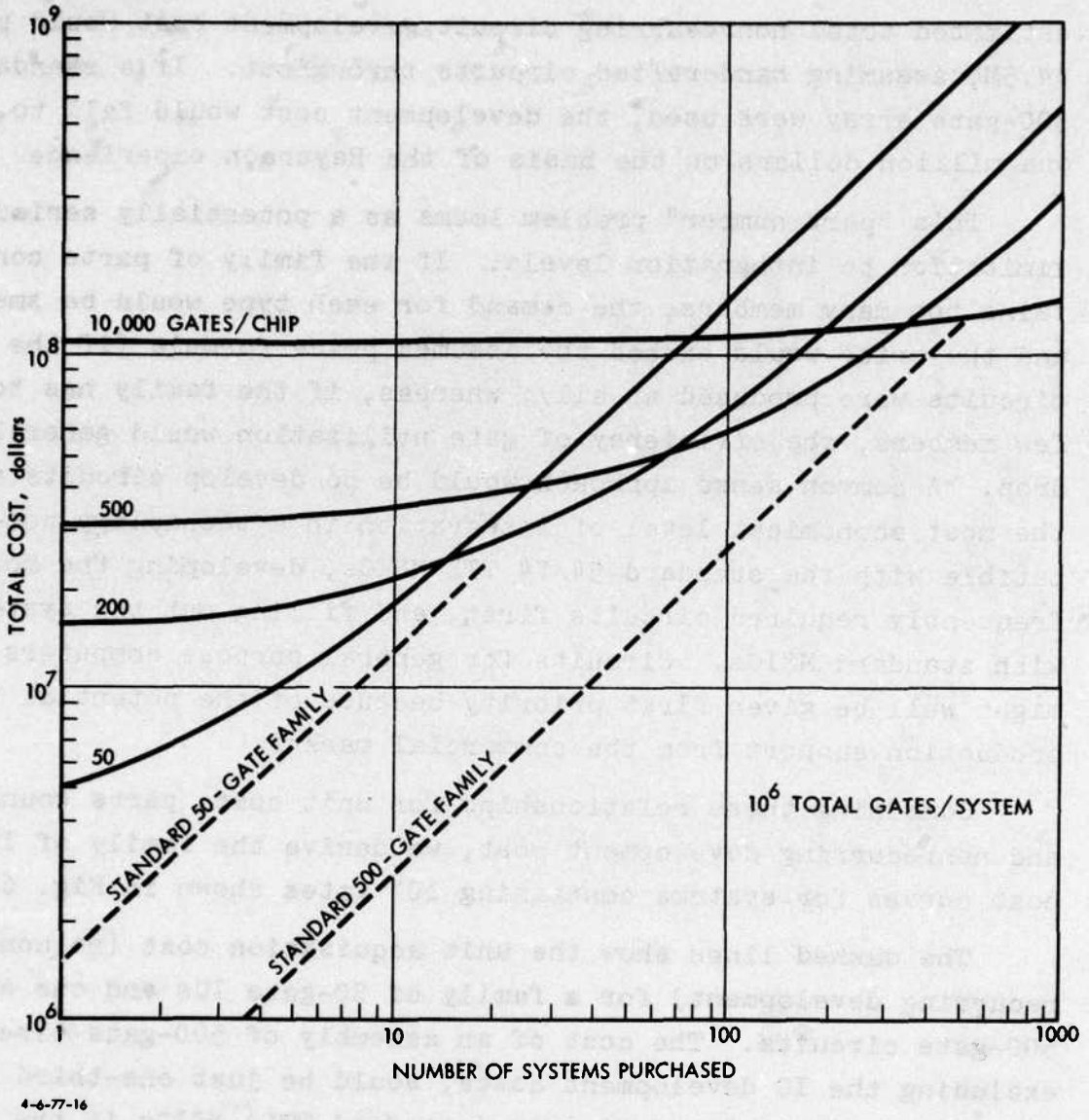

FIGURE 6. Total Cost of Acquisition and Circuit Development

gate family were previously developed, the 500-gate family would only become economical when over 50 systems are being procured.

C. OTHER DIRECT LIFE CYCLE COSTS

Thus far, this discussion has dealt with nonrecurring development costs and the unit production cost of IC assemblies. Consideration must also be given to the costs of operating and maintaining equipment during its operational life, such as the costs of spares and repairs, logistics support, special test equipment, training of maintenance personnel, preparation and updating of maintenance manuals, and so forth.

The out-year costs for spares, repairs and logistics support are directly related to the failure rate of the equipment since this determines the number of maintenance personnel needed for each installation, the number of spares which must be kept on hand, the average rate of repairs or replacement (maintenance transaction), etc.

The failure rate/gate (or per function) of ICs is strongly related to the level of integration because most IC failures (that have not failed in their infancy, Ref. 45) are associated with the mechanical portions of the device--the pins, tabs, connectors, etc.; in more highly integrated circuits, their total number is smaller in relation to the total number of gates, and the failure rate/gate-hour is correspondingly lower. The average failure rate of ICs used here is that formulated by the Rome Air Development Center (Ref. 19) shown in Fig. 7.

The number of spare modules which must be procured and kept in the inventory pipeline and on hand is proportional to the failure rate/gate and to the total logistics turnaround time between the discovery of a failed module and its repair and return to inventory at the operating base. If all failed modules are discarded and replaced with new ones, the turnaround

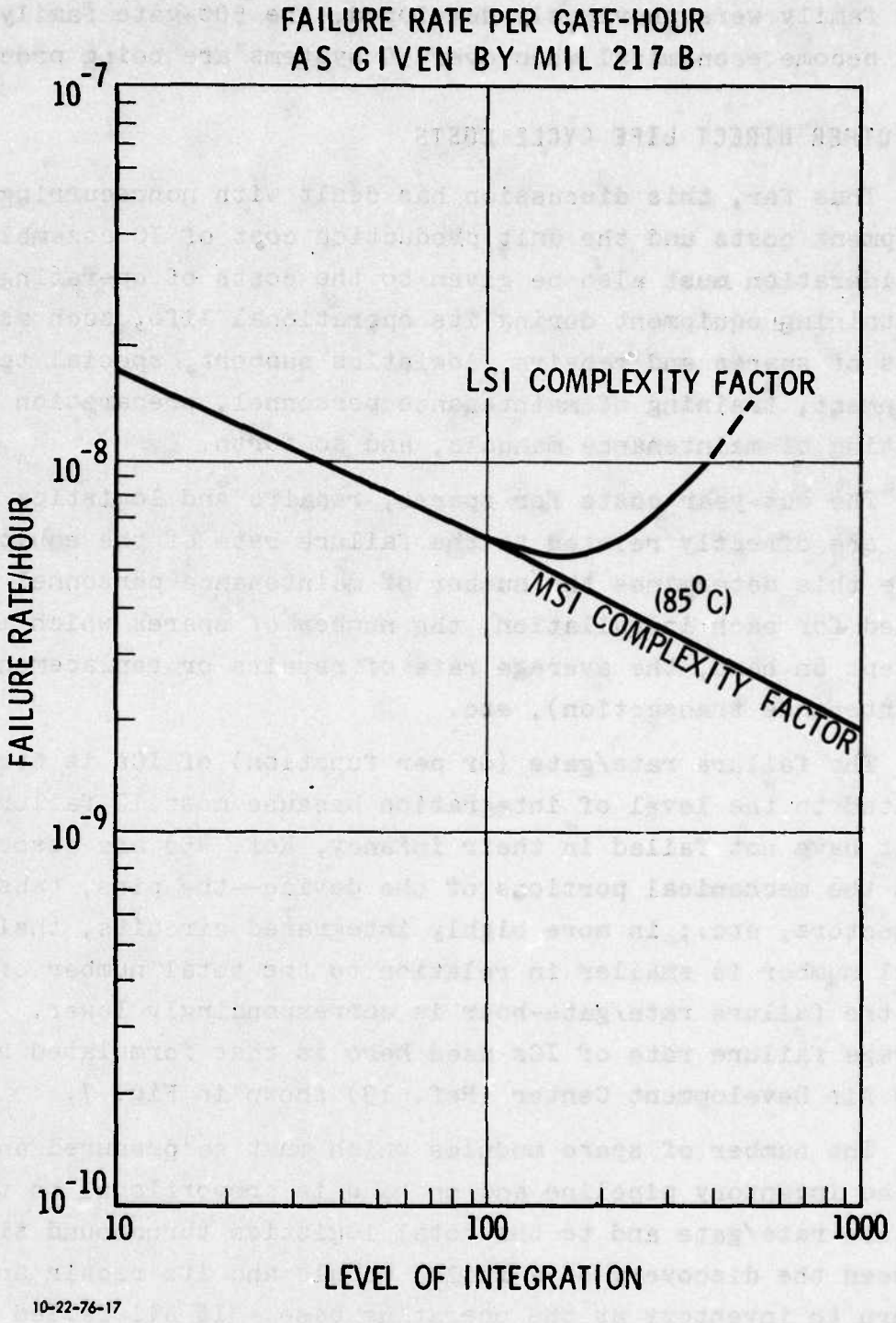
FAILURE RATE PER GATE-HOUR
AS GIVEN BY MIL 217 B
10^{-7}
10^{-8}
10^{-9}
10^{-10}
FAILURE RATE/HOUR
LSI COMPLEXITY FACTOR
MSI COMPLEXITY FACTOR
(85°C)
10
100
1000
LEVEL OF INTEGRATION
10-22-76-17

FIGURE 7.

time becomes, effectively, the total operational life of the equipment. In any case, some fraction of module failures will prove irrepairable, making the effective turnaround time generally intermediate between the two. Since failed ICs (as opposed to modules) are not subject to repair, the effective turnaround time which determines the total number of spares consumed is again the total operating life of the equipment. Symbolic statements of these simple facts appear in Appendix A.

Using representative values for the various parameters, the actual average LCC/gate for spares and repairs has been calculated and plotted in Fig. 8. The slope of this line, which determines the relative cost of two embodiments of the same equipment (at different levels of integration) is greater than the slopes of either the unit cost relation (Fig. 2) or the reliability/gate (Fig. 7) since it compounds the effects of the two.

In a military environment for which the reliability formula (Fig. 7) applies, the LCC of spares and repairs together about equals the unit acquisition cost for MSI levels of integration, but drops sharply and becomes small relative to the acquisition cost at LSI levels of integration. In a protected environment, such as on board a submarine, the mean failure rate--and therefore these costs--are roughly 10 times smaller according to the RADC reliability formula; however, this may be partially offset by a somewhat longer total operating life.

The systems support costs are largely determined during the system design phase when provision must be made to support the IC assemblies. It is during this phase that the use of the higher levels of circuit integration will have the greatest effect on systems costs. However, the performance of an existing weapons system, as it is affected by digital processing, can be upgraded by future retrofits in which more complex assemblies of more highly integrated circuits can be substituted in

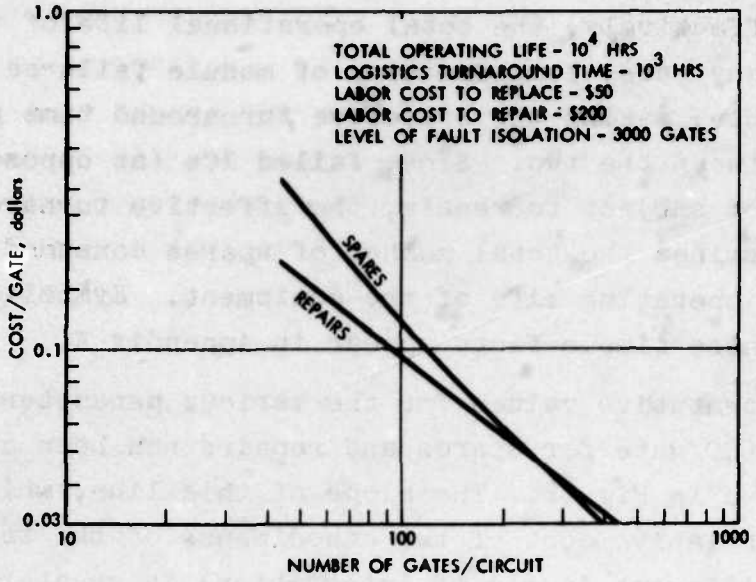

FIGURE 8a. Life Cycle Cost/Gate for Spares and Repairs

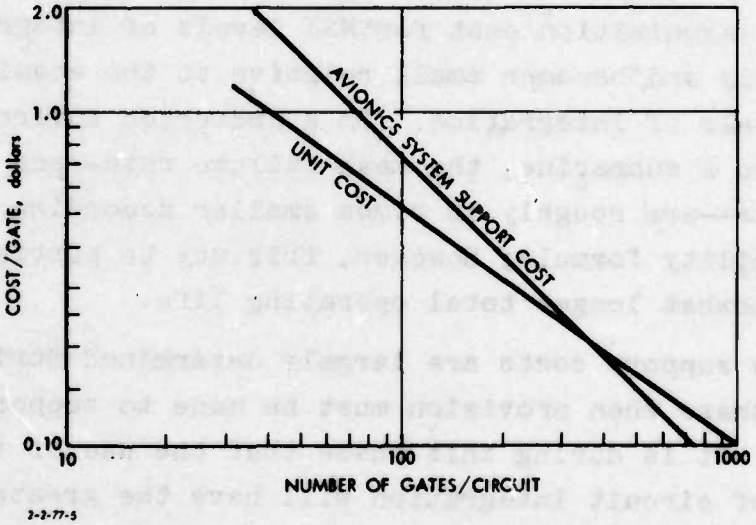

FIGURE 8b. Unit Cost and Avionics System Support Cost (Acquisition)

the same space, using the same power, and dissipating the same amount of heat. Retrofits with improved circuitry are a potential means for reductions in other out-year operating expenses, such as fuel consumption and maintenance; and, the possibility of cost avoidance through retrofitting those systems that are heavy users of IC equipment should be reevaluated whenever significant advances occur in IC technology.

1. Throughput Capacity Per Watt

To the degree that circuit parallelism permits the substitution of a proportionately larger number of slower circuits for faster ones without significant penalty in gate efficiency, the comparative prime power demand for different embodiments of the same logical design depends only on the throughput capacity (number of gate cycles/sec) for the various alternative embodiments. The throughput capacity/watt vs. the level of circuit integration for a half dozen of the most important circuit technologies are plotted in Fig. 9, showing a general improvement in throughput capacity/watt with increased circuit integration as indicated by the dashed line which has been sketched in.

Comparatively, ECL ranks much lower in throughput capacity/watt than it does in throughput capacity relative to cost, since ECL is commonly integrated to a level at which the total heat dissipation reaches several watts; whereas, ICs in other technologies are usually designed to dissipate only a fraction of a watt. Thus, for example, in environments where power is dear, ECL is relatively less economical than CMOS.

D. SYSTEMS SUPPORT COSTS

As remarked upon earlier, the physical characteristics of IC assemblies--such as their reliability, size, weight, and power consumption--directly affect the cost of the host weapons

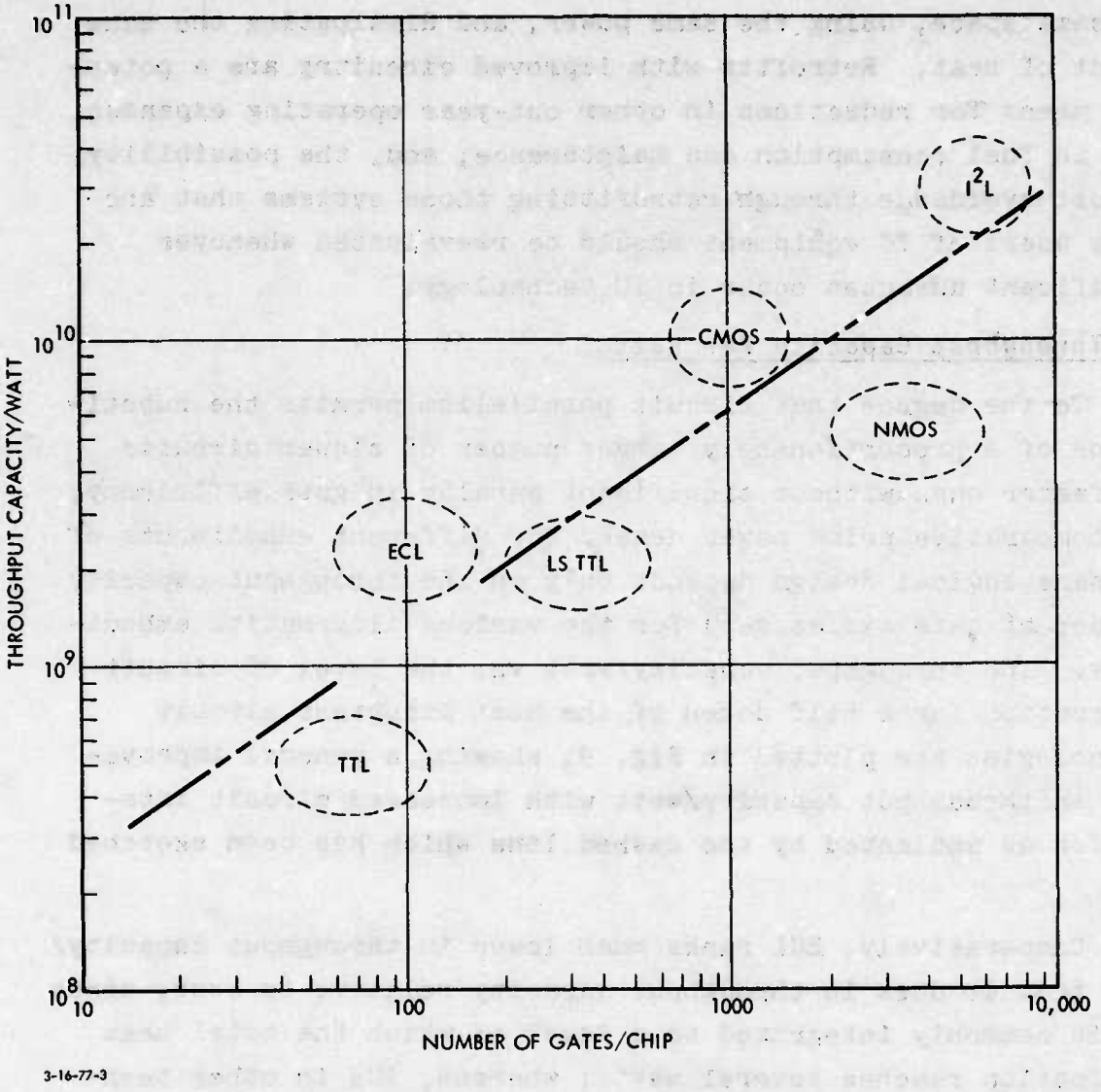

FIGURE 9. Level of Integration. Throughput capacity (number of gate cycles /sec)/watt vs. level of integration

system. The reduction in these costs made possible by the substitution of LSICs for equivalent assemblies of MSICs sometimes overshadows the direct life cycle cost reductions.

A general increase in the level of circuit integration lowers the system acquisition and support costs through its effect on factors such as prime power requirements, air conditioning, fuel consumption, and even the airframe itself, in the case of avionics systems. Together, they lead to a multiplicative effect that augments the impact of economies in size, weight and power consumption of the IC components themselves. The system's overhead multiplier depends on the cost of payload in the weapons system; the multipliers for ships are less than that for tanks, and less for submarines than fighter aircraft, satellites, etc. Any reduction in weight, size and/or power of an electronic subsystem can be applied to weapon-carrying capacity or other military payload; however, the actual value of the space, weight and power consumption saved by the use of more highly integrated circuits is more than the price of the additional aircraft, submarines or tanks needed to provide the equivalent incremental payload, simply because the incremental payload is obtained without actually operating the additional vehicles.

The greater reliability of the LSIC embodiment also raises the availability or operational readiness of the weapons system, which reduces the number of weapons systems units that must be purchased to achieve a specified level of force readiness. An analysis of operational experiences with an A-7D squadron (Ref. 14) showed that the operational readiness of that aircraft was reduced by 10-20 percent because of unscheduled maintenance of its avionics, and that this situation did not improve with experience.

The data in Fig. 9 translate directly into systems support cost for prime power. For example, in a satellite system where (solar cell) prime power typically cost a total of about $2,000/

watt, an I^2L gate that consumes 0.5 mw would contribute one dollar to the total cost of prime power, while a TTL gate of the same speed taking 10 mw would contribute $20. To give another example: An assembly of 300-gate LS TTL gate array circuits would dissipate an average of 6 mw/gate (270 internal gates at 5 mw, 30 driving external circuits at 15 mw), contributing $12/gate to the prime power cost for the system, while an assembly of LS TTL MSICs would average 15 mw, or $30/gate.

1. Weight Per Gate

The weight of an IC assembly also directly affects the systems support cost and it, too, improves with the use of more highly integrated circuits. The weight/gate improves with the level of circuit integration in several ways. For example, the connections made internally in a circuit substrate weigh much less than external connections on or between printed circuit boards; also the weight (per gate) of cabinets, shock mounting, and so on, can be reduced in proportion to the level of integration since the circuits themselves have inconsequential mass; finally the weight (per gate) of the secondary power source decreases with more integration. An IC assembly, including cabinet, printed circuit boards, secondary power and connectors, is about 10^{-3} lb/gate (typically) at the MSI level of integration (30 gates), and decreases almost in inverse proportion to the level of integration. The AN/UYK-30, for example, with an average level of integration of about 200 gates, weighs a little over 10^{-4} lb/gate.

E. AVIONICS SYSTEMS SUPPORT COSTS

Since World War II, avionics have grown in complexity to the point that they now contribute a significant part of the aircraft weapons system LCC (typically 30 percent of both the acquisition and logistics support costs, Ref. 15). They have an important effect on aircraft operational availability

and interact with almost every aspect of the aircraft design (Ref. 4).

During this time, in an effort to achieve continually elevated performance goals, the complexity of the avionics subsystems outstripped progress in component reliability (Fig. 10) with the consequence that the high unit cost and low operational availability of advanced fighters became unacceptable (Ref. 10). As LSIC technology emerged, it was viewed as one means for reversing both the trend towards greater cost and more frequent failures of digital avionics components. However, the rising systems cost, coupled with declining reliability, is a consequence of the "design-to-the-limits-of-technology" approach with can actually feed on improvements in component technology, even where the component reliability and cost are simultaneously improved, as in the replacement of MSICs by LSICs. Suppose, for example, that a 10 lb assembly of 30-gate MSICs consisting of a total of 10,000 gates were replaced, not with an equivalent assembly of LSICs, but with a more complex assembly of 300-gate ICs filling the same space and having the same weight but containing 100,000 gates. Then the unit cost would increase from about $12K to $20K, and the overall failure rate would double (from one to two failures/thousand hours).

THE EFFECT OF SUBSTITUTING LSIC FOR MSIC ASSEMBLIES ON SYSTEMS COST AND RELIABILITY

		LSI Design (300 gates/IC)	
	MSI Design ($) (30 gates/IC)	Equal Performance	Maximum Performance
Number of gates	10,000	10,000	100,000
Weight	10 lb	1 lb	10 lb
Power	150 watts	50 watts	500 watts
Acquisition Cost	$12K	$2K	$20K
Failures/thousand hours	1	0.2	2

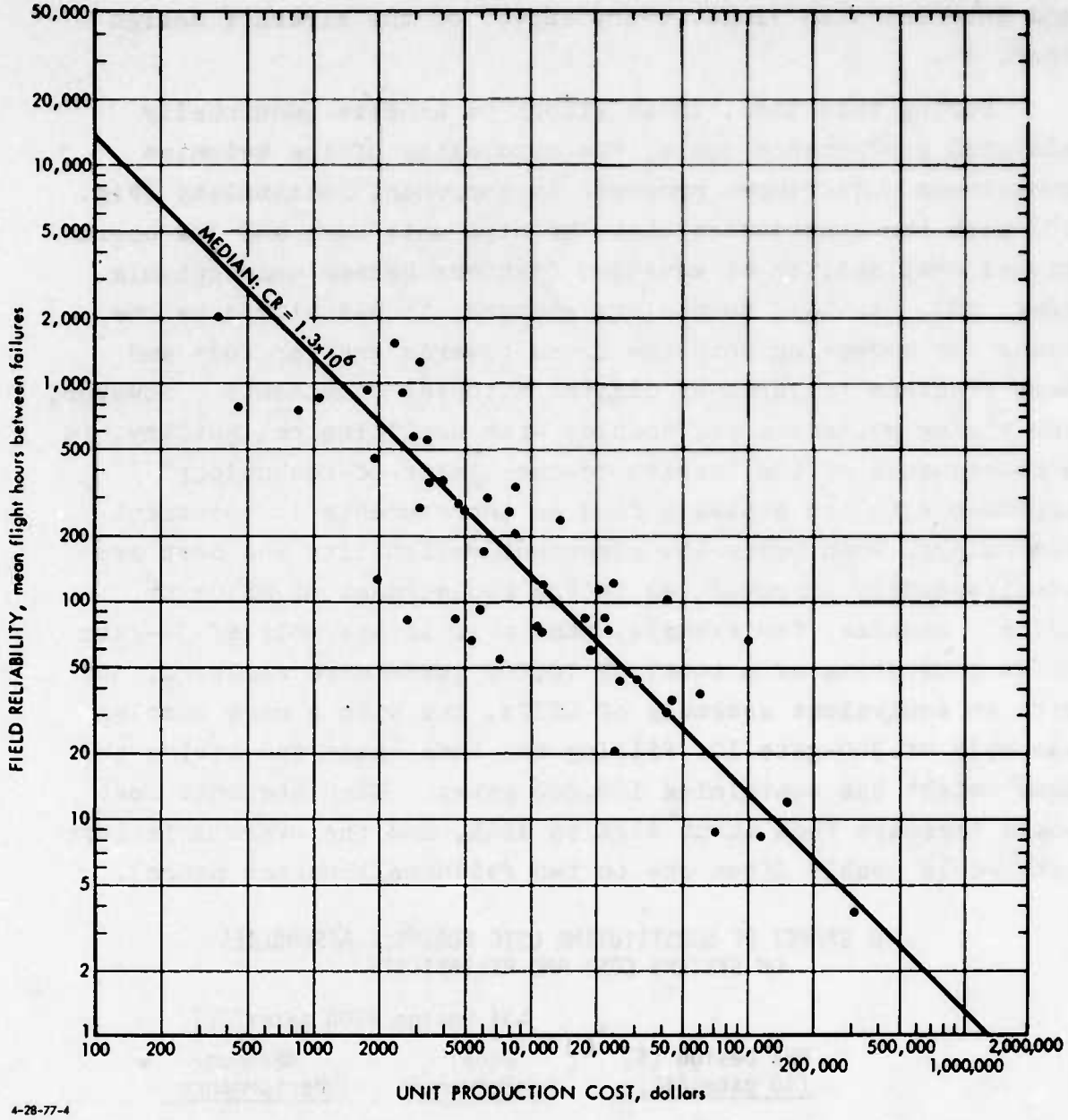

FIGURE 10. Avionics Field Reliability vs. Unit Production Cost. (Ref. 10, p. 59)

Our interest here is in estimating the comparative life cycle systems support costs for two aircraft systems which are equivalent with respect to their operational characteristics, but which carry different embodiments of the same avionics equipment--ICs with different levels of circuit integration--assuming that the two embodiments differ in weight, power consumption and reliability according to Figs. 7 and 9.

Since the mission profile of the two aircraft is the same (by supposition), the greater size, weight and power consumption of less highly integrated circuits would lead to a somewhat larger airframe, larger engines, greater fuel consumption, etc. This is a significant effect in the case of aircraft with heavy electronics complements such as AWACS and E-2C. In the case of these two aircraft, the effect of the avionics particularly requires special investigation into lift, drag, stability and control, control surface response, structural carry-through, assembly and maintainability, although nearly all military aircraft designs show the external effects of their avionics complement to some degree.

A decrease of one lb in avionic weight (or any other fixed equipment) will result in a decrease of 6-8 lbs in "dry" weight, due to the system overhead effect, representing the total iteration of aircraft component weights (fuel, propulsion, structure, etc.). Since the "flyaway" cost/pound of a modern fighter plane is approximately $500, the savings in aircraft cost/pound of avionics weight reduction would average $3500 or so.* The trend in the growth of avionics weight in military aircraft, shown in Fig. 11, is an important contributor to the soaring costs of military aircraft.

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*In 1975 dollars. Some authorities put the figure at $5000 (Ref. 20).

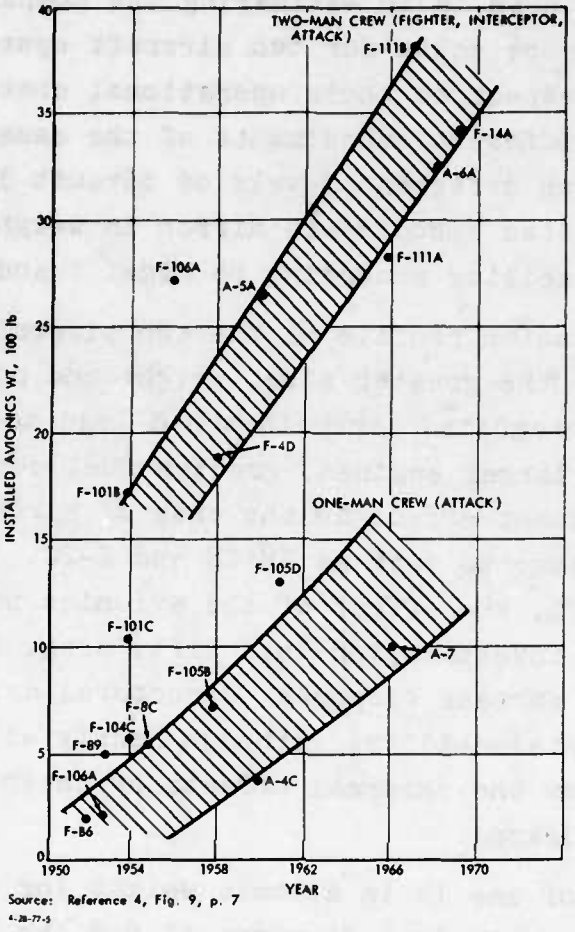


FIGURE 11. Avionics System Weight Trends

The power consumption of avionics also affects the overall aircraft system weight with a similar multiplicative effect because of the added weight of the prime power source, power distribution system, air conditioning, etc. The relationship between the cooling system weight and avionics weight is shown in Fig. 12. It is seen that in the more recent design, the weight "overhead" of the cooling system is about 25 percent of the total avionics weight of the aircraft as shown in Fig. 13. The aircraft generator, which supplies power for the avionics, also adds to the weight overhead and systems cost.*

*It is not surprising that the generators which provide the greatest power in relation to their own weight are also the most expensive relative to their power. For example, a generator which produces one kva/lb costs over $200/kva of capacity, while a unit which produces 0.6 kva/lb costs only $90/kva (Ref. 5).

Taking into account the net effect of weight and power consumption (power supply and cooling), the average net multiplier, G, for modern fighter aircraft is about 6-8 (Ref. 4), and the incremental (marginal) cost, C, of the overall aircraft system associated with the addition of a digital processing unit is given by $C = NGc'Wg$, where N is the number of gates in the unit, Wg the net average weight/gate of the unit and c′ the system "flyaway" cost/lb. If, for example,

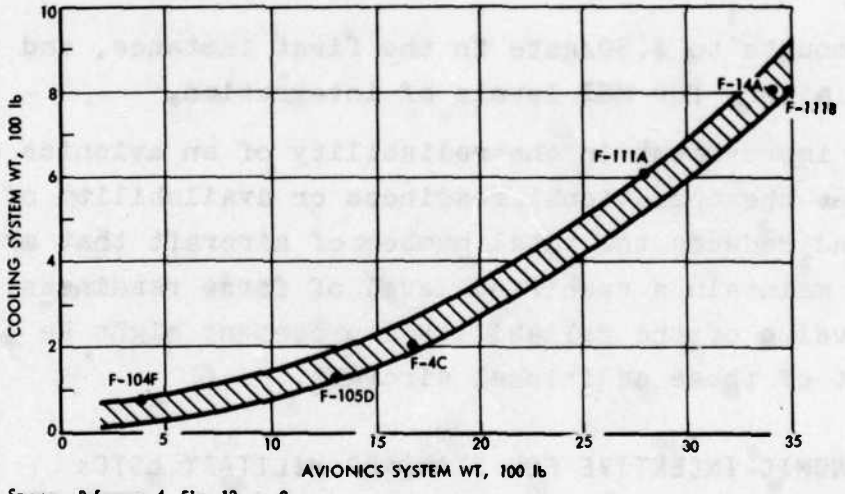
$G = 7$

$Wg = 5 \times 10^{-4}$ lb/gate (standard TTL MSICs)

$c' = \$500$,

then the marginal systems acquisition cost/gate of standard MSI digital processing is \$1.75, which about equals the total direct life cycle cost (Fig. 8a).

The multiplier, G, and the systems cost/lb, c′, will have significantly different values for other types of weapons system carriers (satellites, submarines, surface ships, tanks); for example, the launch cost of satellites range between approximately \$1,000 to \$15,000/lb, depending on the orbit and total payload,



Source: Reference 4, Fig. 13, p. 9

FIGURE 12. Avionics System Cooling Load Requirements

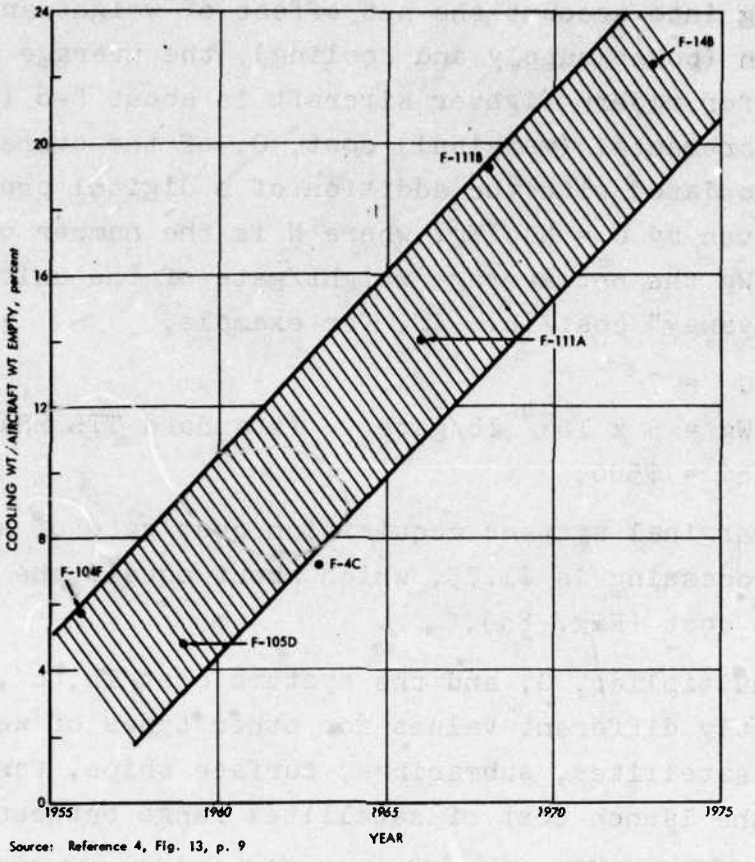


FIGURE 13. Cool System Weight Penalty Trend

which amounts to $.50/gate in the first instance, and $7.50 in the latter, for MSI levels of integration.

An improvement in the reliability of an avionics complement increases the operational readiness or availability of the aircraft and reduces the total number of aircraft that are necessary to maintain a specified level of force readiness. The dollar value of the reliability improvement might be equated to the cost of these additional aircraft.

F. ECONOMIC INCENTIVE FOR STANDARD MILITARY LSICs

At the present time, most military digital processing equipment is built from the 54/74 series TTL MSICs. Several factors account for this: The clock speed is high enough that awkward

multiplexing problems do not arise, a very large variety of circuits are available, the production technology is firmly established and virtually all digital systems engineers are familiar with them and are well-versed in their use. This has been of great benefit to the military and will not, nor should not, change until LSICs of comparable speed and versatility become available.

In this situation, the weapons system program manager and the prime contractor are faced not with the choice of the best level of integration for ICs with which to build a system, but instead whether or not the development of LSICs is actually justified as an alternative to standard TTL MSICs, since the latter involves no IC development with its concomitant risks to the program's cost and schedule.

1. Direct Life Cycle Costs

The direct acquisition cost for IC assemblies, including the nonrecurring circuit development cost, was discussed above (Fig. 6). For a system consisting of 10^6 gates, the development of a family of 200-gate circuits is justified (as compared to the use of standard 50-gate circuits) when the total number of systems exceeds 20, and results in net reduction in acquisition cost of over 60 percent when the number of systems exceeds 100. For 500-gate circuits, break-even occurs at about 30 systems, and the net reduction reaches nearly 75 percent when 200 or more systems are purchased. The unit production costs assumed here are those which apply at commercial levels of production; whereas, a production run of 100 such systems containing 100 different types of 300-gate circuits would require an average of only 3000 of each circuit. It is evident that the indicated unit cost reduction can be realized only if a relatively small family of circuits are identified from which a substantial part of military IC assemblies could be fabricated. The requirement for additional spares for logistics support over the life of the equipment would also contribute to supporting their production.

Table 1 lists a few systems in various stages of development or production which contain appreciable quantities of ICs.

The GPS receivers are still under development and an appreciable part of their total gates will be embodied in LSICs when they go into production. The same is true of the JTIDS receiver, but the BQQ-5 and BQQ-6 will consist of assemblies of MSICs and SSICs.

The systems listed at the bottom of Table 1 also contain appreciable quantities of ICs.

2. Systems Support Costs

The combined effect of the weight and power/gate of IC assemblies on systems support costs are indicated by Fig. 14, where the cost coefficients for weight and power are those discussed in the previous section and the power/gate relative to level of circuit integration corresponds to the trend line in Fig. 9. These would indicate the effect of circuit integration on the F-16 avionics (for example) and the signal processing equipment in the satellite systems. The BQQ-5 and BQQ-6 sonar signal processing systems in their current configuration occupy about 200 sq ft of deck space and dissipate over 30 kw of heat, representing an incremental cost of $\$2 \times 10^6$ or so to the host submarine according to estimates of qualified Naval personnel. This comes to $.20/gate.

The corresponding estimates for systems support costs are listed in Table 1.

3. Logistics, Operational and Support Costs

The level of overall purchase of ICs by the military (currently about $400 million/year and rising at about 20 percent), and the above brief summary of some of the IC requirements and the systems support costs for a few specific military systems, indicates that the total expenditures directly related to IC assemblies will total several billion dollars ($10-20 billion

TABLE 1. ESTIMATED SYSTEMS COST ATTRIBUTABLE TO INTEGRATED CIRCUITS

SYSTEM	PLANNED PRODUCTION	NUMBER OF IC GATES PER SYSTEM	DIRECT LIFE CYCLE COSTS	SYSTEMS SUPPORT LIFE CYCLE COSTS	CIRCUIT SPEED
GPS Receivers	20,000 - 100,000	5×10^3	$60M - 300M	--	1, 10 MHz
BQQ-5, 6	80	10^7	1.2B	$500M	5, 10 MHz
F-16	650	8×10^4	75M	300M	1, 5, 10 MHz
JTIDS Receivers	10,000	10^4	50M	--	1, 10 MHz
Satellite System	10	5×10^6	120M	2B	10, 40 MHz
Others: PATRIOT, AEGIS, F-15, F-18, EF-111, VSTOL, VPX, VAMX, E-2C, AWACS, P-3, etc.					

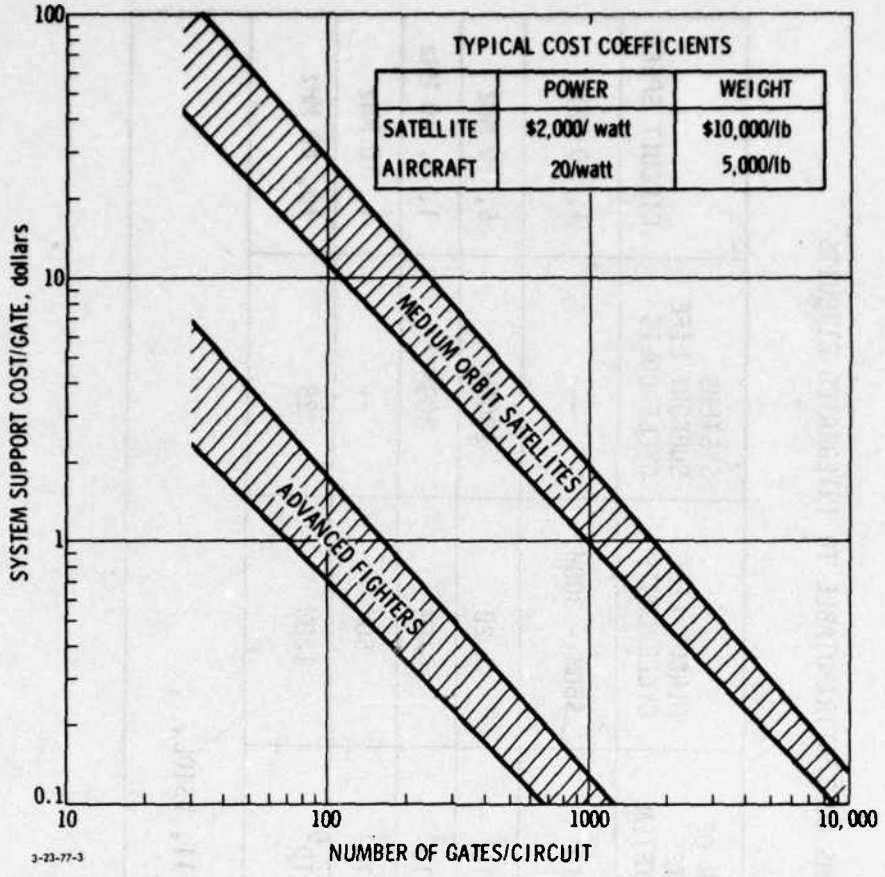


FIGURE 14. Typical System Support Costs for Weight and Power

is a reasonable "guestimate") for those systems now planned or in various stages of development or production. On the whole, these costs appear to decrease about in proportion to an increase in the level of circuit integration. Thus, the introduction of a family of ICs, using the best current technology and standardized on the basis of commonality among all military requirements, could eventually lead to a reduction in these costs approaching one order of magnitude. Of course, the full impact on weapons systems cost would only be felt for IC improvements introduced during the system design phase, when provision must be made for space, weight and prime power.

IV. MILITARY IC REQUIREMENTS

1. The Military IC Demand Spectrum

In order to assess the overall potential for cost avoidance or performance improvements in military IC equipment, we must look first at the circuit characteristics appropriate for these applications and then at the level of circuit integration which is feasible with the applicable circuit technologies. To be sure, military IC speed requirements cover the entire spectrum from the lowest (corresponding to PMOS) to the very highest (ECL, compound semiconductors) speeds. To analyze the economic consequences of a DoD LSIC policy or program, we would have to know the total gate requirements at various speeds--in other words, the demand spectrum.

The information collected during this study permits only a sketchy determination of the military IC demand spectrum in the foreseeable future, and this is summarized in Table 1. However, even from these cases, it is evident that a substantial part of military applications requires medium- to high-speed circuits (10 MHz and higher). These applications include general purpose computers, sonar beam formers, sonar spectral analyzers, speech digitizers and synthesizers, encoders and decoders for error detection, satellite navigation data decoders, radar signal processors, digital autopilots, ELINT analyzers, video data encoders, etc.

2. Performance Characteristics for Military Applications

The current gap between the speed capabilities of commercial LSI microprocessors and military signal processors is indicated by the relative characteristics of the Texas Instruments Advanced Scientific Computer (TI ASC) and the SPS-81, both of which are designed for military signal processing applications, and the INTEL 8080 (one of the most widely used microprocessors).* The IBM Advanced Signal Processor discussed below is comparable in performance to the TI ASC.

	TI ASC	SPS-81	INTEL 8080
Circuit Technology	ECL	TTL	NMOS
Approximate Number of Equivalent Gates	5×10^5	4×10^4	4×10^3
Basic Cycle Time	75 nsec	200 nsec	600 nsec
Multiply Time	75 nsec	1 μsec	1 ms
Word Length	32	16	8

NMOS circuits currently are being produced with about 4000 equivalent gates/circuit and the level of integration with this technology is generally expected to increase steadily, reaching tens of thousands of gates/chip. LS TTL, on the other hand, is currently limited to about 300 gates/chip and ECL to about 100 gates/chip. Higher levels of integration in these technologies is possible in principle by a reduction in the dimensions of the circuit elements and corresponding changes in electrical characteristics which leave unchanged the power dissipation/unit area. (See Appendix D, below.) Notwithstanding the fact that NMOS can be integrated to 20 times the level of TTL and 60 times the level of ECL, in applications which demand the highest throughput rates the use of NMOS is uneconomical (due to its inferior speed relative to cost, as shown in Fig. 4).

*The Texas Instruments Advanced Scientific Computer is designed for use in a computer facility, not a military environment, and a full-blown version of this system, including the huge memory it is capable of handling, fills a large room.

3. Multiplication in Signal Processing

The requirement for large numbers of multiplications characterizes many signal processing applications because of the frequent occurrence of inner product calculations (which consist of the sum of the products of many pairs of numbers). This kind of calculation occurs in filtering, radar pulse compression, encoding and decoding, spectral analysis and beam forming. In fact, multiplication speed generally is so critical that the throughput of signal processors is often expressed in terms of multiplications/sec.

In a "normal" computer, multiplication is generally performed by an algorithm which uses a series of shifts and adds much like the common "pencil and paper" algorithm for multiplication; high-speed signal processors use special parallel multipliers that directly form products using gates only, rather than by a series of additions. There now exist MSI TTL multiplier chips to perform 4 x 4 and 8 x 8 products, and new LSI chips exist to perform 16 x 16 products. These LSI chips use bipolar logic (to achieve maximum speed), consist of thousands of gates, and consume large amounts of power (5.1 watts for the 16 x 16 multiplier); and, special cooling and other mechanical design technologies are needed.

One digital processing algorithm frequently embodied in military applications is the fast fourier transform (FFT). This process involves $\frac{1}{2}$ N $\log_2$ N complex multiplications--N being the number of data points in the transform. In the BQQ-5, for example, 4096 point transforms are computed in 50 ms with 10-bit precision involving 24,576 complex multiplications and additions or one multiplication about every 2 μsec.

4. The Advanced Signal Processor

Several corporations are now developing signal processing hardware and working on signal processing algorithms and system organization. For instance, IBM as developed a new system called the Advanced Signal Processor (ASP) which is scheduled or proposed for use in several military systems.

The ASP provides another excellent vehicle for showing the kinds of speed and complexity required in signal processing. First, because of the high arithmetic load and a need for parallelism in performing signal processing algorithms, a separate microprogrammed "arithmetic processor" is provided with high-speed arithmetic modules. There is also a separate "control processor" that performs conventional system supervisory and data management functions, including the control of the arithmetic processor. The control processor is similar to the IBM 360/370 in instruction word formats, data word formats, and general operation, but the arithmetic processor is specialized in construction. Following are some of the characteristics of both of these processors:

IBM ADVANCED SIGNAL PROCESSOR CHARACTERISTICS

Arithmetic Processor

- Thirty-two-bit word length microprogrammed processor
- Ability to execute special complex function set for signal processing
- Up to four modular arithmetic elements with high-speed working store
- Each arithmetic element contains pipelined 16 x 16 bit-multiplier and 32-bit, three-way adder
- Each arithmetic element is capable of executing 10 million multiples/sec and 20 million adds/sec
- 2K x 69-bit microstore for arithmetic microprograms
- Sine-cosine generator for trigonometric coefficients for FFT

Control Processor

- Microprogrammed, 16/32-bit general purpose control processor
- Ability to execute system supervisory and data management functions
- Three hundred-nsec microinstruction cycle
- Thirty-two-bit arithmetic and logic unit, 5.75-μsec register-to-register multiply
- Sixty-four general registers, 0.3-μsec register-to-register add or subtract
- One hundred and ninety-two external register storage words
- 16K x 34-bits words program store
- 2K x 34-bits words control store
- IBM 360/370-like instruction word format.

The arithmetic processor of the ASP has a modular arithmetic element with up to four units. Each arithmetic unit can execute up to 10 million multiplies/sec and 20 million additions. With two arithmetic units, a 4096-point transform can be performed in about 6 ms and a 2048-point transform in 2.7 ms. This means 166 channels of data could be processed using a 4096-point transform, or 500 channels using the 2048-point transform in an "all out" FFT mode.

When other important military applications are examined (such as voice abstraction and encoding, radar signal processing, message encoding and decoding, the GPS decoding unit, etc.), similar speed requirements are encountered. For example, the speech abstraction section of vocoders using the linear predictive method requires instruction cycles of about 70 nsec (Refs. 50 and 51), and the GPS protected data stream bit rate is 10.23 MHz (Ref. 52). These systems are not likely to be redesigned with more highly integrated circuits (than the standard TTL presently used) unless an LSI circuit technology is at hand that operates at least as fast as the standard TTL. This leads us to an examination of the relative characteristics of the different IC technologies to assess their suitability for medium- to high-speed ICs.

V. LSIC TECHNOLOGY CONSIDERATIONS

A. CIRCUIT CHARACTERISTICS OF LSICs

A large number of transistor types have now been developed and utilized as individual components, but only a very small subset of these are candidates for LSICs because of the severe restrictions inherent in the production technology and the geometry of such devices.*

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*Some of these restrictions are:

- In isoplanar circuits, where transistors are formed on the plane surface of a single crystal silicon wafer, the transistors and interconnections are formed of parallel planes of various materials including layers of silicon of controlled impurity content, insulating materials such as silicon dioxide, and metals for electrode interconnection, all parallel to the wafer surface and with their lateral dimensions determined by photolithographic methods.

- Processing requires exposure of the wafer surface to a sequence of operations of great sophistication, typically including oxide film formation, etching of numerous openings in the oxide film at locations precisely defined by photolithography, chemical treatment of the exposed surface, heat treatment to diffuse impurities into the wafer, further oxide treatment and photolithographic exposure, further chemical treatment to apply other types of impurities, further heat treatment for diffusion, reoxidation and reexposure, application of metal by vacuum evaporation in patterns determined by photolithography, etc. Each process step must be designed to not interfere deleteriously with prior steps.

- Since many wafers (each identical, and each having typically several thousand transistors on it, elaborately interconnected) are processed simultaneously; extremely high standards of production control of each process step is required if yield is to be high enough for practical purposes. Only by restriction to the most reliable processes and the simplest device forms can acceptable yield be readily obtained.

There are a number of different basic classes of circuit types and several designs for each type of IC. In general, the ICs we now use can be divided into two broad categories:

a. Bipolar. These ICs utilize conventional junction transistors in which the three electrodes of a triode structure are separated by pn junctions.

Bipolar transistors have high transconductance even at low operating voltages because of their stacked parallel plane geometry, and low interelectrode capacitances, compared to their operating currents. Because of this, they operate at switching speeds of the order of one nsec, and even at this speed, they are usually limited by circuit considerations rather than transistor characteristics.

Bipolar transistors have the distinguishing characteristic that clouds of charge carriers comprising the useful output current must pass through a base electrode populated by larger numbers of carriers of opposite charge without a large proportion of the carriers disappearing by mutual recombination. This is impossible in most semiconductors; practically only silicon and germanium permit this kind of operation and then only if "recombination centers," crystal defects and certain types of impurities, are kept to a very low concentration. Thus, bipolar transistor performance is greatly affected by the bulk properties of the semiconductor, and affected relatively little by surface properties under ordinary conditions.

Impurity concentration, especially in the thin base electrode of a bipolar transistor, tends to be critical and is

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• Components must be limited in operating power dissipation to avoid necessity for elaborate cooling provisions. If LSI is to be achieved, logic circuits such as ECL, which inherently achieve high-speed performance with large power consumption/gate, must be ruled out, or used sparingly in combination with other low-power components.

difficult to control during manufacture without special precautions. A too-low impurity concentration is conducive to collector-emitter breakdown, while too high a concentration eventually results in collector-base breakdown.

The historical progression of major bipolar ICs has been: Resistor-Transistor-Logic (RTL), Diode-Transistor-Logic (DTL), Transistor-Transistor-Logic (TTL), Emitter-Coupled-Logic (ECL) and Bipolar Diffusion (BD). The latest major circuit line in the bipolar arena is Integrated Injection Logic (I^2L). The Schottky clamp is often used in bipolar circuits such as TTL and I^2L to increase circuit speed.

b. MOS Logic. MOS devices are field-effect transistors (FETs) and do not require the interpenetration of free-charge carriers of opposite sign, so that semiconductor type and quality requirements can be relaxed as compared to bipolar transistors. There are three major types of MOS now in use; these are PMOS, NMOS and CMOS. However, there are many variations and new techniques in development or existence and much discussion and work on DMOS, CMOS on SOS (silicon-on-sapphire), VMOS, and others is taking place.

In contrast with bipolar transistors, MOS devices have much lower transconductance because the depth of the stream of charge carriers comprising the useful output current is much smaller than that of a bipolar transistor. The useful current of a bipolar transistor flows broadside to the plane of the electrodes; the current of an MOS transistor flows from the edge of the source electrode and is collected at the edge of the drain electrode. The depth of the sheet of current in the conducting channel is seldom much more than one micron, and is often less.

The threshold bias of an MOS transistor depends sensitively on the chemical potential of the surface film on the semiconductor between source and drain and underlying the gate electrode. This chemical potential is sensitive to traces of contaminants during

production and to the thermal and electrical history of the device. Trace quantities of mobile ionic impurities, such as the alkali metals and the halogens, can cause change in the threshold bias during life, at room temperature, and must be rigorously excluded from the production environment.

While sensitive to surface contaminants, an MOS transistor is much more tolerant of bulk property variation of the underlying semiconductor than is a bipolar transistor. MOS transistors can and have been formed of many other semiconductors than silicon and germanium; one important type, the "silicon-on-sapphire" MOS transistor, is constructed of silicon deposited epitaxially on sapphire crystal. Since the two crystal lattices do not match precisely, the resulting silicon film is too full of defects to permit efficient bipolar operation, but is usable for MOSFET devices, with the advantage of low electrode capacitance and, therefore, greater speed.

The small current and low transconductance of MOS transistors, together with the fact that their electrode capacitances are nearly as large as those of bipolar transistors, means that MOS devices tend to be much slower than bipolar devices. Their compensating advantages are their simplicity and consequent high production yield, and their small size and low power/transistor, which permit use of large numbers on one chip without thermal problems. The low power consumption of MOS devices makes them well suited to portable, battery-powered devices. One family of MOS logic circuits, the CMOS family, draws power only during switch transitions and, hence, has a power requirement that varies directly with clock speed. CMOS was developed for space and ocean work and has very low standby power, making it attractive where devices are required to function only on an intermittent, infrequent basis. As the rate at which CMOS circuits change their states or toggle increases, however, CMOS consumes more and more power until, at about a three-MHz rate, it consumes as much power as low-power TTL.

CMOS/SOS designates a circuit technology in which the silicon substrate is grown epitaxially on a synthetic sapphire crystal. This technique attacks the problems of slowness in MOS circuits; and, after years of effort, production devices are now being introduced. However, some semiconductor groups have abandoned their CMOS/SOS development efforts, while others are experimenting with alternative techniques for achieving the same end (see, for example, Ref. 59).

c. A Systems Designer's View of IC Technologies. From the systems designer's viewpoint, several comments can be made concerning the major circuit lines now being offered. First, TTL has had the greatest usage in military systems. It is fast, has moderate packing density for bipolar circuitry and there are many different circuit combinations available in packages. TTL has been approved for military usage and there are modules (boards) available that are also approved, so a designer can begin work at once and have a large supply of parts available. The designer need not worry about supplies, and the circuit characteristics are well known from both an electrical and a logical viewpoint; therefore, large arrays of TTL circuits can be designed with confidence. There are numerous computer programs on logic design available as design aids to the system (programs to help layout front panel wiring, for instance), and technicians can construct and debug TTL circuit configurations with assurance. The standardization and "MIL spec-ing" of TTL have helped its popularity. TTL was and is an excellent technology for implementing computer designs.

The major problems with TTL concern its low packing density and high heat generation/gate. These two factors are the major reasons why TTL cannot be used in LSI. There are, however, variations in the basic TTL gate which are used in MSI, and these circuits are also available in MIL spec modules.

The fastest commercially available logic that is widely used is ECL: it has delays of less than one nsec/gate, making it faster (by a factor of about 4) than TTL. Designers tend to shy away from ECL because (1) interconnection of ECL circuits is difficult and wiring layouts must be carefully made, and (2) ECL is power-consuming and cooling can be a major problem for large arrays.

Despite ECL's problems, it is used in most of the newer "super" (super-large, superfast) computers because designers need the speed and are "willing to pay the price" in order to compete in the commercial market. ECL is used far less in military applications because of its low packing density, the elaborate cooling schemes required, and noise problems (it is considered to be noise sensitive). It is known to be difficult to use, that the circuits require much work to debug, and that obscure problems arise with interconnections; these are additional hindrances to greater use of ECL.

Since for both ECL and TTL the level of integration is limited to 100 gates or less by the power dissipation/gate, low-power bipolar technologies have been sought. This search has produced low-power Schottky TTL (LS TTL), I^2L, and SFL devices. LS TTLs maintain the medium-speed capability of TTL but require only 2 to 3 mw/gate (internal), which allows the level of integration to be increased to several hundred gates.

The circuit topology of low-power Schottky TTL is very similar to that of standard TTL. The major difference between these two technologies is that in LS TTL a Schottky barrier diode is connected between the base and collector of the transistors in a Baker clamp configuration (Ref. 27). This diode prevents the transistor from entering saturation during circuit operation and reduces the turn-off time that results from saturation-caused charge storage. This enables higher speed operation to be attained at lower power dissipation levels. Correspondingly, except for

the addition of the Schottky diode, the fabrications processes of LS TTL are quite similar to TTL processing procedures, which are mature and well-established. In addition to this, LS TTL can very effectively utilize advanced processing techniques, such as small geometry device layouts and shallow diffusion processing. These techniques will permit the achievement of greater device density and increased chip complexity. Another advantage of low-power Schottky TTL is its electrical and functional compatibility with all forms of TTL. This is important, because many times it is desirable to utilize TTL memory, control, and peripheral circuits to supplement the microprocessor chips.

B. COMPARISON OF RELATIVE PRODUCTION FEASIBILITY OF LSIC LOGIC OPTIONS

At present, there are several types of circuits and logic gates which are known to be feasible for LSI on a monolithic silicon chip; Table 3A summarizes from one manufacturer's point of view (Ref. 36) the more important characteristics of the several types of logic families which are now, or may soon become candidates for LSIC systems. Other promising candidates and components are known but have not yet been developed to the degree necessary for confident evaluation (e.g., DMOS). Technical progress in the LSIC field has been so rapid that this table will probably require revision within a year or so. On the other hand, many older logic families, such as RTL and DTL, are virtually obsolete and are not included.

The intricate detail and complexity of LSICs make computer design aids essential in order to arrive at a satisfactory production design.

First, the idealized logical operations of the device can be simulated on a computer and checked out and debugged. Then the actual circuit elements, including realistic capacitances

TABLE 2. SUMMARY OF TYPICAL LSI CHARACTERISTICS

	CLOCK	POWER PER GATE	POWER-DELAY PRODUCT	GATE DELAY	NUMBER OF GATES PER CHIP	THROUGHPUT CAPACITY		DENSITY GATES/mm^2
						PER WATT	PER CHIP	
TTL	5 MHz	10 mw	100 pJ	10 nsec	75	5×10^8	4×10^8	40
LS TTL	10	5	30	6	300	2×10^9	3×10^9	40
I^2L	5	0.15	1	4	4000	3.3×10^{10}	2×10^{10}	250
ECL	50	20	20	1	100	2.5×10^9	5×10^9	30
PMOS	0.6	2	200	100	4000	3×10^8	2.5×10^9	150
NMOS	3	0.5	20	60	4000	6×10^9	1.2×10^{10}	200
CMOS	3	0.3	10	30	1000	10^{10}	3×10^9	40

TABLE 3A

DESIGN TECHNOLOGY	LAYOUT COMPLEXITY	TEST AND CHARACTERIZATION	PRODUCTION	PACKAGING
Bipolar				
TTL	100-500 gates/chip	Easy	Easy	Easy, well known
TTL, whole wafer	3000 gates/ wafer	Moderate	Very difficult	Difficult
I^2L	1000-5000 gates/chip	Moderate	Moderate to difficult (two-level metallization required for high complexity)	Difficult
ECL	100-200 gates/chip	Difficult	Difficult (two-level metal)	Easy to difficult
MOS				
CMOS	200-2000	Moderate (depends on function, random logic difficulty, design dependent)	Easy for bulk CMOS: SOS & hardening difficult	Easy
PMOS	1000-5000	"	Easy	Easy
NMOS	1000-5000	"	Moderate to difficult	Easy

and operating conditions, can be simulated for the individual gates and subsystems to assure realization of the idealized logic design. Interactive computerized graphic displays substantially aid the designer, but fully automated layout of the required gates, interconnections and circuit elements on the silicon chip is the most difficult computer design task, and programs are not available for many types of LSICs. Such programs that do exist usually require extensive manual assistance from an operator. One automatic system has been developed for one type of logic, CMOS, but revision of the resulting design by a human operator can typically make a 20 or 30 percent improvement in gate efficiency.

The status of these and other computer aids to LSIC design are shown in Table 3B. A final design test is usually performed by connecting the prototype to a simulator and exercising all functions of the chip. Some of these programs also partially localize any single fault which occurs, such as a "stuck" gate. This is what is meant by "graded single fault" testing in Table 3B; the term "graded" relates to the partial localization as distinct from precise localization in a particular transistor or other circuit element.

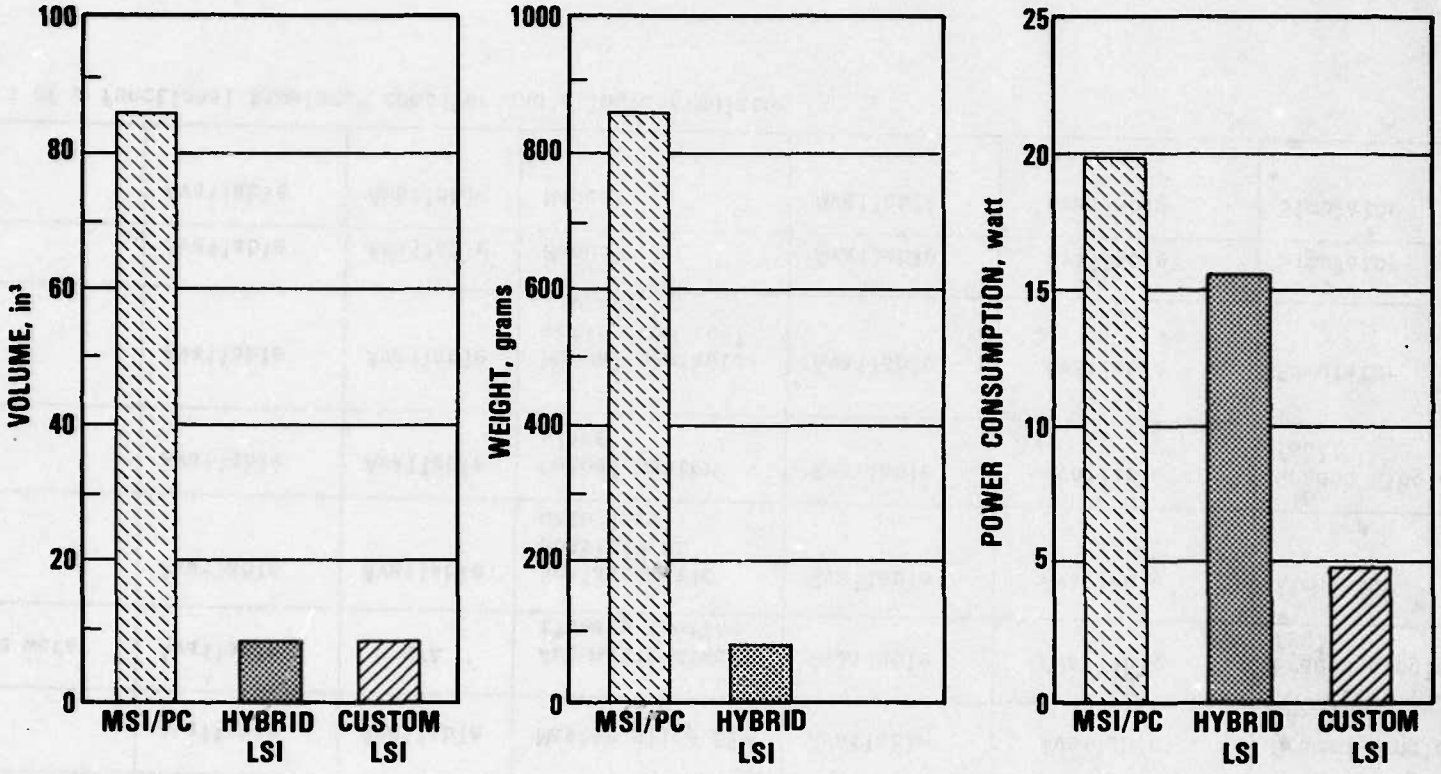
C. HYBRID ASSEMBLIES

The hybrid assembly of MSIC and SSIC components interconnected, packaged together, and hermetically sealed is sometimes used as an alternative to the development of a custom LSIC. The reduction in weight, volume and power consumption of the hybrid, as compared to a printed circuit board assembly, is illustrated by a specific example in Fig. 15. The resulting weight and volume compare well with an equivalent LSIC design, but the hybrid exhibits only a small reduction in power consumption and little reduction in unit cost compared to conventional printed circuit boards.

TABLE 3B

	DIGITAL* SIMULATION	CIRCUIT ANALYSIS	AUTOMATED LAYOUT AIDS	INTERACTIVE GRAPHIC EDIT	LAYOUT VERIFICATION	TEST
T^2L	Available	Available	Master slice SEM	Available	Available	Graded single fault
T^2L whole wafer	Available	N/A	Automatic discretionary routing	Available	Available	Graded single fault
I^2L	Available	Available	Semiautomatic possible at gate level	Available	Available	Simulator
ECL	Available	Available	Manual master slice	Available	Available	Graded single fault
CMOS	Available	Available	Manual semiautomatic from cell library	Available	Available	Simulator
NMOS	Available	Available	Manual	Available	Available	Simulator
PMOS	Available	Available	Manual	Available	Available	Simulator

*Consists of a functional simulator compiler and a logic simulator



Source: Westinghouse

4-7-76-61

FIGURE 15. NADC Pulse Train Separator

The production of hybrid assemblies is not a simple matter. MSI chips are frequently damaged during assembly; corrosion can cause gradual deterioration of interconnections because "hermeticity" (perfect sealing) is difficult to assure. Integrity and control of beam lead bonds to substrates require refined techniques. In summary, great care is necessary to design durable and economical hybrid structures; nonetheless, those manufacturers who have perfected the manufacturing technology regard the hybrid assembly as an economically attractive alternative to the conventional printed circuit board construction.

D. ADVANCES IN IC PRODUCTION TECHNOLOGY

Much emphasis has been placed on the physical and economic advantages associated with higher levels of circuit integration and also on the nonrecurring cost and risk involved in IC development. Both of these factors continually motivate the IC manufacturer to search for new production techniques.

Currently, most ICs are manufactured by a photolithographic process in which a photographic mask is placed over the chip--sometimes in immediate contact with it--and then exposed to ultraviolet light to form a pattern in the photoresist, which coats the chip. The areas of the photoresist that are exposed to light are made either soluble or insoluble to the developer. Thus, a patterned layer is created in preparation for a subsequent step of etching, plating, diffusion or ion implantation.

The practical extent to which the size of the circuit elements can be reduced is limited by the optical resolution of the lithographic process, registration errors in successive masking operations, irregularities in the surface (flatness variations) of the wafer, and light scattering.

For example, in an optical projection system using a perfect f/2.0 lens, diffraction of light would place a limit on the resolution at about 2μ, but the depth of focus of the projection lens

would not equal the flatness variation of silicon wafers and this would limit the practical line width to 5μ.

Electron beam (E-beam) lithographic techniques are the object of numerous experimental and developmental programs aimed at improving the physical quality of ICs and possibly also reducing development costs (Ref. 37). In E-beam lithography, the desired pattern in the photoresist is formed by scanning an electron beam by driving the beam-deflection circuitry from a stored program pattern generator. In E-beam lithography, the electron beam takes the place of light and the stored program--used to drive the deflection coils or electrodes--replaces the mask. Because, fundamentally, E-beam lithography has greater resolution and depth of focus than optical lithography, it is possible to produce circuits with smaller gate structures and higher levels of integration. E-beam lithography under stored program control is particularly convenient for producing chips that contain a ROM section, which must be coded differently at the factory for each user. In the mask-making process itself, the limit of optical resolution degrades the mask quality and ultimately contributes to loss of yield; for that reason, E-beam pattern generators are already used in the production of masks. The E-beam pattern generator can make chromium master masks not only with better accuracy but also with better linewidth control and edge quality, lower defect density, at lower cost and with faster turnaround (Ref. 38).

The E-beam lithographic process can only be carried out in a vacuum, which means that the chip must enter and leave the system through a decompression chamber. Furthermore, the alignment of the chip can no longer be done visually--by the manipulation of a microscopic stage--but must be performed automatically by the use of secondary electron emission from special indexing structures on the wafer. Finally, because of the sequential nature of patterned beam deflection, the process is

intrinsically slow; any attempts to speed up the process by using higher beam currents degrade resolution because of space charge beam spreading.

Nevertheless, the process has been perfected and is currently being used to produce I^2L devices. Over 100 chips are produced on a single wafer and each lithographic step takes a few minutes for the entire wafer. At the end of each exposure, the wafer is removed from the apparatus through the decompression chamber and the photoresist is developed.

E-beam lithography for IC production promises to pay off in (1) higher yield by producing improved masks for the present photographic method, (2) lower cost and reduced lead time in the production of custom LSICs through the elimination of photographic mask development, and (3) reduced device size with higher levels of integration.

The reduction in circuit size achieves two major benefits: a sharp decrease in the unit cost of circuits and a corresponding increase in circuit speed. The relationship between device size and speed is discussed elsewhere in this paper, but suffice to say the smaller linear dimensions result in lower gate capacitance, shorter transit time of holes and electrons in the semiconductor, shorter interconnect lines (with correspondingly lower capacitance) and so on.

At the writing of this report, an experimental projection E-beam system is being built and evaluated at Naval Electronics Laboratory Center by W. R. Livesay (Refs. 39, 40).* In this system, a photo cathode is first prepared having the desired line pattern in the form of photo emissive material to the same scale as the IC. In the process of exposing the chip (which is

*The system described in Ref. 39 gives 1μ lines with a 0.2μ precision over a 250-mil square chip.

first coated with an electron-sensitive photoresist), the photo cathode is flooded with ultraviolet light, causing electrons to be emitted from the line patterns, which are then focused on the chip. This method eliminates beam scanning, making it proportionally faster.

VI. DETERRENTS TO THE UTILIZATION OF LSICs IN MILITARY EQUIPMENT, AND INSTITUTIONAL CONSIDERATIONS

A. DETERRENTS

1. Development Cost and Risk of Overrun

Although the manufacturing technology for both bipolar and field-effect circuits--such as ECL, TTL, LS TTL, NMOS, PMOS, CMOS--are well-established, the design and development of new ICs at high levels of integration carry the risk of layout defects (which prevent the circuit from operating at the design speed) and design errors (i.e., not embodying the intended logical design). The engineering design team and the design verification process consume much of the budget and schedule. Because of the penalty--in schedule slippage and cost overrun--incurred when redesign is necessary, the top-tier design teams (usually consisting of a half dozen or fewer people) are regarded as important assets by the semiconductor manufacturers; they are generally reserved for work on those ICs that promise the largest gross sales in the form of IC units or end products. The manufacturers, as a group, probably see little incentive to apply their best design teams to the development of custom circuits for military needs.

Advances in circuit design technology such as automatic design computer software, software-driven mask preparation, and E-beam lithography may eventually bring substantial reductions in the cost and lead time of new chip developments. The immediate prospects appear particularly promising for I^2L devices.

The use of gate arrays for embodying new circuits, which involves only the final metallization, reportedly reduces development time to eight weeks, typically with a correspondingly sharp dip in cost.

A joint-service DoD program to develop a standardized military LSIC family could have the effect of removing the risk from the program managers and distributing the costs and risks of custom circuit development over many weapons systems developments, while consolidated IC and end-product purchases would make the development of dedicated military circuits more attractive to the semiconductor manufacturers.

2. Technology Obsolescence

Some of the early circuit technologies, such as TRL, DTL and HLDTL, were perfected and replaced by other technologies in approximately five years; new technologies, such as DMOS, VMOS and SFL, are currently under examination. In contrast, weapons systems usually have an operational life of 20 years, and sometimes more. This raises the question of whether or not sources of new spares and replacements will be available over the operational life of the system; a particularly vexing aspect is that the proven shelf life for these devices is not yet comparable to the scheduled operational life of the systems. Furthermore, if one type of IC technology were superseded and its production terminated, the succeeding technologies may require different power supply voltages, which could add considerably to the cost of a retrofit in the new technology.

However, even if deployed units used circuit technology which eventually becomes obsolete, IC manufacturers would undertake the production of devices for spares and replacements,

provided the size of the run justifies the cost of re-establishing manufacturing process control. The National Security Agency (NSA), for example, consolidates its purchases and maintains production of silicon-gate NMOS SSICs at an economical level.

If military customized LSICs are utilized in major weapons systems, DoD must be prepared to contend with possible technology obsolescence through measures which facilitate replacement--such as interface standardization, module standardization and federated power distribution--in other words, through design for retrofit. Or, if these fail, DoD must make the commitment to sustain production in the old technology through consolidated purchasing.

3. Cost of Qualification and Documentation

The process of qualification and documentation to military standards deters the high-volume production-oriented semiconductor manufacturer from bidding on military LSIC development, particularly since the usual method of government procurement separates development from production contracts. These costs also make custom IC development less attractive to the program manager.

The cost and duration of qualification programs are alleviated by adopting qualification procedures, such as accelerated life testing, qualification of assemblies rather than components and qualification of processes rather than circuits.

This deterrent, like the nonrecurring development cost, is mitigated by distributing the cost over many weapons systems.

4. Logistics, Special Test Equipment and Training

The proliferation of highly complex sophisticated electronics equipment in military systems (due to the unbridled

pursuit of performance without a proportionate consideration for the problems of operational and logistics support) has resulted in almost prohibitively expensive systems which, in many cases, have less than satisfactory records of operational availability (Refs. 1, 10 and 14). In the carrier task force with strict limits on space (for maintenance personnel, special test equipment and spare parts) the operational support problems have apparently reached near-crisis proportions.

As a consequence, the unscheduled maintenance and logistics delays associated with electronics equipment false-fault determination, etc., have become major contributors to the loss of operational availability.

Standardization is a means for reducing the number of different part types and the variety of different test equipment. In the case of LSICs, greater reliability is obtained and throwaway costs are reduced.

B. INSTITUTIONAL CONSIDERATIONS

1. The IC Manufacturers

a. Retention of Gross Sales. Advances in production technology (process control) have raised the IC yield to the point that circuits now come off the production line "like popcorn." In a highly competitive industry, this creates a favorable environment for perennial price warfare, which would consign the semiconductor manufacturers to a perpetual low profit status, to the benefit of their OEM (Original Equipment Manufacturer) customers. Some of the semiconductor managers foresaw, well in advance of the event, that in perfecting their manufacturing process they were sowing the seeds of their own financial undoing as OEM suppliers. They began the process of vertical integration into the end product business

(the production of digital watches, hand calculators, TV games, etc.). By the same logic, the continuing invasion of the minicomputer field by the IC manufacturers becomes inevitable. However, the principal avenue to the capture of military gross sales (the supply of military systems) is not accessible to most of the semiconductor IC manufacturers. The military systems suppliers, with in-house dedicated IC facilities (such as Raytheon, IBM, TRW and Westinghouse), have taken the lead in exploiting this opportunity.

b. Pricing Policy. The managers of the IC manufacturing corporations cannot now be expected to cooperate enthusiastically in the decimation of their own gross sales by offering $100 LSICs that do the job of $1000 worth of their present MSICs. Rather, unless induced to do otherwise by government procurement policies and competitive pressures, the semiconductor manufacturer would be motivated to offer the bipolar LSIC at a premium because of its intrisically superior speed, reliability, and the indirect cost benefits.

If the government is to share substantially in the potential savings from the use of more highly integrated circuits, special procurement policies (such as consolidated procurements) need to be devised and adopted. These policies would have to provide for large enough orders to insure competitive bidding and also give the semiconductor industry incentive to apply its talents to supplying the government LSIC needs by making (for example) the market for entire digital processing subsystems directly accessible to the semiconductor manufacturers.

c. The Pros and Cons of Government Contracts. The semiconductor industry, like its underlying technology base, changes rapidly. When production proceeds at a high and sustained rate

manufacturing profits are good. This encourages keen competition for high-volume production orders; but, when demand slackens, the intense competition makes it impossible to protect profit margins, which magnifies the impact of normal economic cycles on the semiconductor industry. The manufacturers respond to this as best as they can (e.g., by dropping unprofitable product lines, sometimes without notification, which alarms weapons systems program managers whose requirements for ICs are relatively canonical (owing to the long operational life of major weapons systems)).

To the extent that military weapons LSIC requirements actually proceed independently of the cyclical commercial demand, they would represent an attractive market; but, IC manufacturers complain that the low volume of typical military purchases, together with requirements for second sourcing, special qualification, documentation (and contractual separation of development from production), are a hindrance to the effective utilization of LSICs in military equipment.

To be sure, many commercial LSICs now appear in military equipment (such as the AMD 2900 in the AYK-14 and the INTEL 3000 in UYK-30) and are of unquestioned value. Yet even these circuits are criticized as having a mechanical design unsuited to many military applications, and their uncertain continuing availability over the projected operational life of these equipments is a source of concern.

In sum, the general low degree of commonality between the interests of the LSIC suppliers and the DoD casts doubt on the viability of any DoD policy concerning LSICs that depends on the IC manufacturers as suppliers.

2. Military Equipment Suppliers

The suppliers of military equipment and weapons systems understand well the military requirements for ICs and the

economic and performance incentives for utilizing advanced IC technology, but, in most cases, they do not have the LSIC design teams to translate these requirements into a family of customized IC chip designs. In many instances, they have developed digital processing equipment on a proprietary basis as a means of obtaining sole source orders, but few of the suppliers have undertaken high-speed LSIC designs on this basis.

Among those in the industrial sector, the military equipment manufacturer is the most responsive to the needs of the government, particularly when these needs are clearly expressed in the form of criteria for contract awards. One of the most effective means for eliciting the beneficial application of LSIC technology to military systems would be for military program managers, systems project offices, GFE development groups, etc., to write their specifications in terms that motivate the supplier to examine the potential benefits of advanced technology LSICs as an alternative to the use of standards MSICs--taking into account out-year costs and problems.

3. DoD Management

The problems which appear to impede a fuller utilization of advanced technology LSICs in military equipment are the sort which are dealt with at the managerial level in the private sector, namely, establishing policies (the basis for contract awards, acceptance of risk), dealing with out-year costs, imposition of standardization, allocation of responsibility (as between program managers and GFE development groups), etc.

For example, standardization is well recognized as a means for reducing nonproductive and costly proliferation of

types of equipment. The problem is the classic one of realizing the benefits of standardization without inhibiting the introduction of valuable new technology--"Don't throw out the baby with the wash water." In the private sector, this issue is being faced and standardization policies are being set down at the management level (e.g., Texas Instruments on software compatibility and Westinghouse on data busses and modularity).

VII. LSIC DEVICE TYPES

A. MICROPROCESSORS AND THEIR USES IN EXISTING SYSTEMS

A microprocessor is generally taken to be a Central Processing Unit (CPU) for a computer which is in LSI and consists of one chip (or at most, a few). The microprocessors now commercially available are mostly in NMOS or PMOS, but an I^2L design recently announced by TI and a few CMOS chip sets are also available.

Because of the popularity of the term "microprocessor," some manufacturers call their processor assemblies "microprocessors" even when they require quite a few chips and are built entirely of standard MSI TTL circuits. This leads to some confusion as to microprocessor capabilities because these designs are relatively fast (TTL speeds). Furthermore, some manufacturers offer microprogrammed processors, generally in MSI TTL or even ECL, which they refer to as "microprocessors."

As levels of circuit integration increase due to the development of more compact circuit forms and the use of larger chips, it has now become possible to create an entire computer on a single chip by including enough ROM and RAM to store programs and data. These are usually referred to as "microcomputers."

One example where hardwired TTL logic was directly replaced with a microprocessor can be found in the Army's AN/UGC-74 Communications Terminal. This is a small militarized terminal with a keyboard and display (printer), along with connectors

for interfacing communications links using a 188C interface, other terminals, test sets, etc. Figure 16 shows a block diagram of this system. The original design included several boards in a small replaceable module which was connected to the printer, keyboard, and communication interface convertor using a special board inside the terminal but not in the module.

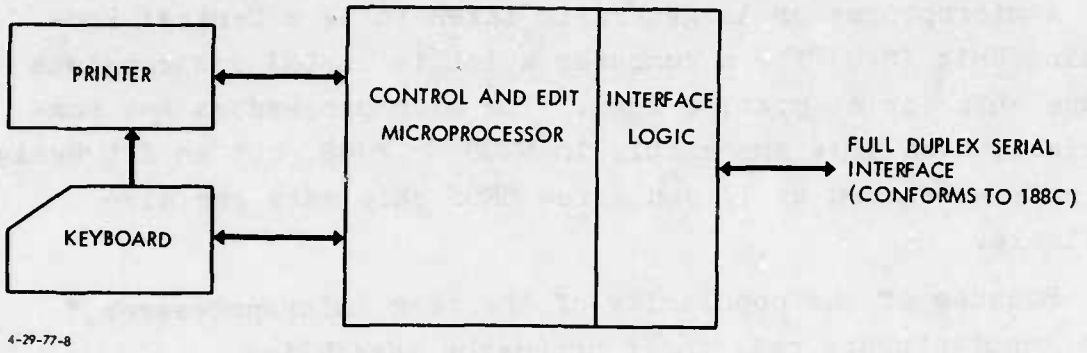


FIGURE 16. AN/UGC-74 Teletypewriter

The new design directly replaced the old module in size, electrical and mechanical connections, and included a commercial INTEL 8080 microprocessor with 4K words of RAM, 10K words of PROM and two boards of input-output drivers. The new module can perform the additional functions of message composition, editing, prompting and buffering. A list of the monitor commands appears in Table 4; the editor commands are in Table 5. The printer speed attainable was increased from 150 to 600 words/min, transmission over communications links is provided at up to 1200 words/min and either ASCII or the Baudot code may be used.

TABLE 4. AN/UGC-74 MONITOR COMMANDS

KEY SEQUENCE	ACTION OF MICROPROCESSOR
600 Test	Invokes test pattern printing
Transmit	Transmits message in compose area
Print	Prints message in receive area
Move	Moves message in receive area to compose area
Delete	Deletes message in compose area
R Delete	Deletes message in receive area
L Set	Sets printer line length to 80 columns
S Set	Sets printer line length to 72 columns
Edit	Invokes text editor subsystem to initiate edit commands

TABLE 5. AN/UGC-74 EDITOR COMMANDS

EDITING COMMAND	ACTION OF MICROPROCESSOR
B	Moves file pointer to beginning of message
E	Moves file pointer to end of message
M (±) DD	Moves file pointer up (-) or down (+) by DD lines
T (±) DD	Types DD lines starting at file pointer up (-) or down (+)
D (+) DD	Deletes DD lines starting at file pointer
I	Allows insertion of lines into message, until control Z
S# String #	Searches for character string between delimiters (#) and moves file pointer to line containing string
R# String 1# String 2#	Searches for String 1 and replaces with String 2
P	Invokes prompting software subsystem

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LARGE SCALE INTEGRATED CIRCUITS FOR MILITARY APPLICATIONS.(U)
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This work was done by the Communications/Automatic Data Processing Laboratory at the request of the Project Manager, Army Tactical Communications System. The use of the INTEL 8080 microprocessor was based on an approach developed at the Naval Electronics Laboratory Center using basic building blocks developed there.

This replacement of the conventional hardwired logic with the microprocessor-driven system shows a direct example of an application area when LSI can replace conventional logic. In this case additional features were added to the system, but a functionally equivalent replaceable unit would have been possible. The new unit that was developed is operable with all previous units and can be directly substituted in all existing systems. Furthermore, the newly developed module can replace existing modules, if desired.

Another very similar development is a Submarine-to-Satellite Information Exchange System (SSIXS) Subscriber Terminal developed at the Naval Electronics Laboratory Center, San Diego, California. This terminal uses an 8080 microprocessor, and a bus design was made, along with a board, which has been offered as a candidate for the Standard Electronics Module (SEM) Program. This terminal is plug-to-plug compatible with a previous system but includes some additional functions. Again, this is an example of an application area--terminals--where state-of-the-art microprocessors can perform satisfactorily, and where direct substitution of plug compatible systems using microprocessors is often possible.

The above two terminals and the many terminals that now use microprocessors of the INTEL 8080 or Motorola 6800 types utilize LSI MOS technology and provide examples where LSI is easily applied. The key factor is the slow speeds at which printers, keyboards and communications links operate. Interfacing electromechanical devices is another area where LSI MOS microprocessors are now being frequently used because of the low speeds necessary

in most cases. A less obvious characteristic is that these applications require few arithmetic calculations and thus do not press the present-day microprocessors' lack of multiplication and division instructions.

The use of microprocessors and microcomputers in military systems, when higher speeds are required than can be provided by the "conventional" commercial chips, generally centers around the use of microcomputers that have been fabricated using MSI chips. These chips generally use TTL for the high speed that is obtainable.

An example is the Raytheon RP-16, a microcomputer which has been used in a number of military systems. The RP-16 is packaged in a 6" x 8" module that can hold up to 48 16-pin DIPs, along with up to 60 discrete components. A two-sided printed circuit board is used and the module meets MIL-E-16400 or MIL-E-5400. The components used meet MIL-STD-38510 or parts vendor-screened to MIL-STD-883-B.

The microprocessor can run up to the 10-Mc (or more) clock rate needed in many military applications. It is, however, not LSI in the sense of the MOS LSI in the INTEL 8080 or the Motorola 6800, since it uses low-power Schottky TTL logic for its speed. Over 16 applications of the module are now in existence and Table 6 lists some of those to date.

B. BIT SLICES

We have seen that the maximum practical level of integration for the faster bipolar technologies is limited by the ability of an individual circuit to dissipate heat (within its operating temperature range) relative to the average power/gate. For LS TTL (ECL), the average power/gate is 2 to 5 mw*

*15-mw TTL gates are needed to drive output lines (tabs, pins, connectors, etc.)

TABLE 6. APPLICATIONS OF RP-16

PROJECT NAME	APPLICATION DESCRIPTION	SYSTEMS COMMITTED	SYSTEMS HARDWARE		SOFTWARE CODE (est) LINES
			AU/CU	MEMORY	
SPS-49	Shipboard antenna control	1 prototype	1	6K	6,000
SQS-56 Follow-On	Sonar display processor	12 products	1	32K	8,000
IEWS Signal Sorter and System Controller	ECM signal processor/ system controller	1	2 3	17K 53K	5,000 20,000
Flight Mission Simulator	Patriot missile flight simulator	1	1	10K	7,500
Project 611	Sonar data processor	4	1	6K	5,500
C-Band Lightweight Acquisition System	Radar track and search processor	1	2	8K	5,500
Sea Sparrow Software Maintenance Facility	Peripheral device controller	1	1	16K	8,000
Interactive Tabular Display System	Display controller	1	1	16K	3,000
TPQ-31	Radar target tracker	2	2	18/256 x 16 Bipolar	800
Hostile Weapons Locator	Search processor, track processor	1	4	8 1K x 16 Bipolar 4 256 x 16 Bipolar	4,000
NRL Software Center	ECM signal sorter processor	1	3	4 4K x 16 NMOS	8,000
Transportable Surface Radar	Radar signal processor	1	2	6 1K x 16 Bipolar	5,500
Shipboard F/C System Test Ted	Weapons system simulator	1	3	4 1K x 16 Bipolar 2 256 x 16 Bipolar	2,500
SCAT	Sonar display processor	1	1	2 4K x 16 NMOS	3,000
Design-to-Price	ECM display processor	4	4	8 4K x 16 NMOS	4,000
SQS-56	Sonar display processor	4	4	8 4K x 16 NMOS	8,000
Marine Collision Avoidance	Radar signal processor/ display	1	1	6 2K x 16 Bipolar	10,000
Space Shuttle Command Encoder/ Decoder Brassboard	Data communications modem and tester	1	2	2 4K x 16 NMOS 1 2K x 16 NMOS	8,000
IEWS Self-Assembler	Software development processor	1	3	4 4K x 16 NMOS 4 2K x 16 NMOS	12,000
NATO Sea Sparrow Software Verify Test Center	Weapons system simulator	1	1	6 1K x 16 Bipolar	5,000
Ka Band Receiver	Receiver signal processor	1	1	1 4K x 16 NMOS	2,000

and the levels of integration cannot exceed 300 gates (100 gates) without the use of special cooling techniques. By comparison, a 16-bit microprocessor requires a few thousand gates. This would indicate the need for using as many as 15 (40) different circuits to construct a 16-bit processor using these technologies (such as the Raytheon Missile Born Computer, which is assembled from 15 300-gate arrays of six different types).

The bit-slice concept is a circuit design innovation by which processors can be assembled from bipolar components while the number of distinct IC types is minimized. In the bit slice approach, entire portions of the processor are divided or "sliced" into identical sections in such a way that each slice is devoted to the processing of (usually) two or four bits in the word.

The chips are interconnected to form a processor, and the division of capabilities is such that word sizes, address length and, in general, register lengths and data path widths are expandable. Thus, an arithmetic element (ALU) may be formed of chips, each of which can input or output 4 bits, then a 16-bit adder, shifter, subtracter, etc., can be formed of 4 chips, while an 8-bit ALU would require only 2 chips. Lateral connections between the slices provide for ripple carry in arithmetic and bit shift and rotation operations.

> The bit slice concept was an important innovation since continuing the MSI route by offering parallel processing or a larger arithmetic unit in a package would give only a slight improvement in the gate to pin ratio and would actually decrease the effective packing density. In the bit slice approach, this horizontal organization is done away with in favor of a vertical organization which combines on one chip different functional blocks that otherwise operate on several chips. All of the blocks on one chip operate on the same data. The current bipolar bit slice circuit, such as the INTEL 3000 series or the Monolithic Memories 5700/6700 or the Advanced Micro-devices 2900 or the Fairchild Micrologic all operate with microinstruction executions at the rate of 5 to 10 megahertz.

> However, the features that make bit slice so attractive to the sophisticated user--that is, the flexibility and adaptability--make it also more difficult to support with applications information. But properly used and understood, in conjunction with high performance bipolar ROMs and PROMs, this bit slice approach may offer an economical, compact and reliable alternative to standard SSI and MSI allowing the designer to concentrate his efforts on a higher, more meaningful level of imaginative systems design. At the present time, almost every digital circuits engineer is familiar with the standard TTL MSI family of the circuits and can use them effectively, but relatively few engineers are versed in microprogramming. However, this situation is changing and in the next few years, many of these engineers will become proficient in the writing of microinstructions. [Reference 17.]

Commercial bit-slice LSICs comprise the essential elements of the AN/AYK-14 (which uses the AMD 2900 series) and the AN/UYK-30 (which uses the INTEL 3000 series).

C. MICROPROGRAMMABLE BIT SLICES

Microprogramming is an old term in the computer industry and has been discussed and used for about a quarter of a century. The "inventor" of microprogramming, M. V. Wilkes, described it as an orderly way to design the control element of a computer.

In microprogramming, the control signals (which activate register transfers, counters, signals, peripherals and so on) cause the system to perform the set of operations constituting an instruction and are stored in a special memory that is read out and applied to the control lines in response to an execution command. This contrasts to the alternative approach in which clock pulses, cycle counters, opcodes, etc., are applied to a network of logic gates which, in effect, "computes" the control signals. The microprogram method reduces the number of gate delays and speeds up the operation by minimizing the number of memory fetches and achieving the highest level of parallelism in the processor and other functions.

When the microcode (the actual microprogram instructions) is accessible to the user, the system is said to be microprogrammable.

In microprogrammable machines, the designer selects his own set of machine instructions subject to constraints imposed by the wiring of the control network; this is why the term "variable architecture" is often used to describe microprogrammable systems. These are stored in PROMs. Then, the selection of sequences of microinstructions and loading them into the PROM replaces (in a hardwired embodiment) the translation of the logical design into a set of interconnected IC modules and the PC board interconnection layout.

Because of the availability, speed of operation, and low cost of ROMs, microprogramming lately has become increasingly popular, and books and papers concerning this subject now appear in quantity. Microprogramming is used in the new IBM computers, DECs PDP 11 and many of the other new designs.

An important fact concerning microprogramming is that the programmer, who is said to be "microprogramming," writes programs which directly control the registers and memory of the computer. An assembly-language program is written in a "higher level language" than a microprogram and has the advantages generally associated with higher level language.

Microprogramming is often used in computers which emulate or imitate other computers. Some computers (such as Burroughs B/1700) are specially designed and particularly good at emulation, and there are several commercial computers that are sold as microprogrammed computers and consist of sets of registers, control inputs for register interactions and a ROM facility for controlling the system.

Most processors made of slices are microprogrammed and the microprogram controller, or sequencer, is formed of slices in the same way the ALU is formed. This concept may be extended to input-output chips, memory buffer chips, etc. Most major IC manufacturers now produce a sliced microprogrammed chip set for users who require higher speeds than can be obtained using the "conventional microprocessor" although these chip sets are often called microprocessors.

The bipolar bit-slice IC offers the advantages of LSI to a number of applications, such as intermediate performance minicomputers, signal processing, etc., that would otherwise require a few hundred TTL MSI chips. The bipolar bit-slice chips commonly use Schottky bipolar or LS TTL technology with a few hundred gates/chip and 40 to 50 pins.

VIII. A STANDARDIZED MILITARY LSIC FAMILY

One approach for achieving a more effective utilization of LSICs in military equipment is the delineation and development of a family of standard circuits based on commonality among the various military IC equipment requirements. This approach addresses nearly all of the issues relating to the utilization of advanced LSIC technology that have been raised in this study and previously by others (Refs. 22, 23, 24, 25 and 28).

A standardized family of circuits using advanced medium- and high-speed circuit technology would make the benefits of the highest practical level of circuit integration accessible to all military equipment designers. By channeling military demand into the minimum number of different circuit types, the highest production rate would be sustained and hence, the most economical unit cost of production. The investment in special test equipments, training, and documentation would be minimized (compared to an uncontrolled proliferation of circuit types) and the cost of circuit development, qualification and documentation would be distributed over the maximum number of equipments and systems. Individual program managers and systems project officers would be relieved of the risks and investment involved in new circuit development. As designers familiarized themselves with these circuits, the cost and program risks would decline. In other words, standardization is a means of bringing the benefits of circuit integration to military equipment while minimizing the deterrents and making the military IC business more attractive to IC manufacturers.

To be useful and effective, standardization requires the attention and active intervention of management (in the case of DoD, a joint services program). In any case, standardization that is too rigid probably would be counterproductive in the long run, particularly when applied to a rapidly evolving technology such as ICs. (In this connection, the standardization programs adopted by individual companies merit study.) Standardization need not be made mandatory provided individual deviations can be justified. Furthermore, the standards themselves might provide for future retrofits when more advanced technology makes this desirable. And, standardization need only apply at the functional level, leaving semiconductor manufacturers free to introduce new circuit technology and designs (such as functional parallelism).

In any case, the development of a standard family would be productive only to the extent that it fulfilled a fairly exacting set of conditions* including speed, physical integrability, completeness, efficiency of gate utilization, compatibility and applicability.

1. Speed

Most of the military computers, signal processors, encoders and decoders, etc., consist of assemblies of TTL MSICs which operate at clock speeds of about 10 MHz. In principle, the same throughput can be achieved by paralleling lower speed circuits through full-speed multiplex circuits, but this would

*The LSIC industry has grown in a few years to total sales exceeding $500M/year, chiefly from the sale of microprocessors, ROMs, RAMs, programmed logic arrays, bit-slice processors, and so forth. These circuits have proved to be of sufficient flexibility and universality that they satisfy the requirements of many users whose aggregate demand creates sufficient volume to maintain production at efficient levels. The identification of circuits having a demand curve which intersects the LSIC cost production curve was a crucial step in the growth of the LSIC industry.

probably require more redesign effort than would an embodiment with high-speed LSICs.* This is not to say that all military IC requirements could be met with 10-MHz components. Experimental vocoder and radar systems, for example, are being built of 60-MHz ECL chips (Ref. 26).

2. Completeness

The family of military customized LSICs should comprise a reasonably complete set of the necessary building blocks for the various types of military digital processing units; however, full compatibility with the 54/74 series of ICs is advisable in any case.

3. Efficiency of Gate Utilization

The efficiency of gate utilization in a design depends, to some degree, on the skill of the designer. Generally speaking, the gate utilization would be better using ICs at lower levels of integration (MSI) rather than higher (LSI), with hardwired rather than programmable designs, and with microprogrammable (variable architecture) rather than fixed microinstruction systems. Any overall increase in gate count in an assembly of LSICs designed to replace an equivalent assembly of MSICs would lessen the actual improvement in costs and physical characteristics discussed in Section III.

4. Compatibility

For efficient gate use, it is often necessary to use MSI memory control, peripheral circuits, etc.; therefore, unless the military customized family of LSICs were compatible with the standard 54/74 TTL MSI family, it would be necessary to redevelop a large number of those circuits. This would delay the transition to the new circuitry and add unnecessary cost.

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*ICs consisting of high-speed multiplexing and demultiplexing circuits (in ECL, for example) and lower speed paralleled circuits (in I^2L)--on the same chip--would be functionally indistinguishable from high-speed series circuits; however, they would have a somewhat poorer gate efficiency.

5. Applicability

To realize the cost benefits of more highly integrated circuits and give adequate inducement to the semiconductor manufacturers to compete for production of the military ICs, the demand for each member of the family must remain at a high level. This will hold true to the degree that each circuit is widely applicable, and particularly if a commercial market developed that would help support production.

6. Irreducibility

The smallest set of circuits meeting these qualifications would be best with respect to logistics and unit cost.

IX. FINDINGS AND SUGGESTED DOD LSIC PROGRAM OPTIONS

A. FINDINGS

This study finds that cost reductions or performance improvements approaching one order of magnitude may be possible through the use of more highly integrated circuits in the digital processing portions of military systems. Additionally, the findings indicate that IC technology itself is not an obstacle, but that a group of problems remains to be dealt with relating to digital systems engineering, commonality and standardization, DoD Management and procurement policies.

1. Life Cycle Cost (LCC) Reduction

Estimates of the LCCs of military weapons systems attributable to IC equipment, excluding the nonrecurring development cost of the ICs themselves, indicate the possibility of cost avoidance totaling several billion dollars over the next 10 years by introducing more highly integrated circuits in military equipment which would otherwise require the standard 54/74 series of transistor-transistor logic (TTL) circuits.* The calculated savings are about equally divided between the direct costs of digital processing equipment (including acquisition and maintenance), and the system support costs--which consist of all of the marginal costs of carrying and supporting the digital processing equipment within the weapons systems or intelligence gathering system.

a. Direct LCC. The direct LCC reduction would come from lower unit production and maintenance costs due to the greater

*This family of ICs is described in Ref. 13.

reliability of more highly integrated circuits, such as LSICs with a few hundred gates each, as compared to an equivalent assembly of standard MSICs with an average of 30 to 50 gates each.

b. Systems Support LCC. The lower weight, size and power consumption of assemblies of more highly integrated circuits contribute to lower systems acquisition and support costs (through their effect on prime power supply, air conditioning, airframe weight, fuel consumption, etc.), while greater reliability raises the availability or operational readiness of the weapons systems and reduces the number of weapons systems units which must be purchased to achieve a specified level of force readiness.*

The reliability, size, weight, speed, power consumption and marginal production cost/gate all improve with higher levels of integration brought about through changes in semiconductor technology or circuit design. These factors reduce the average power/gate relative to speed (power-delay product).

Calculations of the approximate direct LCC reductions from the use of more highly integrated circuits indicate that, with a level of integration of a few hundred gates and clock speeds of 10-20 MHz, savings of one or perhaps two billion dollars might have been effected in systems already under development if current IC technology had been available when they were designed. If systems support costs are included, the potential for cost avoidance in all military IC equipment approaches $10B over the next decade. Alternatively, IC improvements might be applied toward correspondingly higher performance within the weapons systems, rather than to cost reductions.

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*Unscheduled maintenance and logistics delays attributed to avionics systems significantly reduce the operational availability of some currently deployed aircraft (Ref. 14).

In the medium-speed range (10 MHz) and at the level of integration of 300 to 500 gates, circuit technologies such as LS TTL, I^2L, a combination of LS TTL and I^2L on the same chip, are well established* (Refs. 17 and 29).

The established military weapons systems programs that might benefit most by the introduction of more highly integrated circuits, if their deployment schedules would permit, include BQQ-5, BQQ-6, GPS, E-2C, AWACS and JTIDS.

2. Deterrents to the Introduction of New LSICs in Military Weapons Systems

At the present time, there exist serious deterrents to the introduction of custom LSICs in weapons systems. These include the costs of circuit development, qualification and documentation; the uncertain future availability of new circuit technologies (technological obsolescence); the costs for special test equipment and training of maintenance personnel, and the proliferation of device types, which add to the cost of logistics and increase the probability of systems nonavailability because of logistics delays.

Deterrents of an institutional nature include the risks perceived by the program managers to schedule, program cost and out-year logistics support; the unattractiveness of the special military IC market to the semiconductor manufacturer, and the lack of policy at the DoD level as it relates to standardization, procurement procedures, etc., conducive to utilization of advanced-technology LSICs.

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*The INTEL 3000 series Schottky bipolar microprogrammable two-bit slice devices, for example, operate at 100 nsec microinstruction cycles and contain a few hundred gates. The Fairchild 9400 LS TTL also operates at 5-10 MHz microinstruction rates and consists of four-bit slices.

3. Universal Military Standardized LSIC Family

The great potential for cost avoidance afforded by more highly integrated circuits (finding #1 above) and the considerable deterrents to the use of custom ICs (finding #2 above) suggest that consideration be given to the development of a family of medium-speed, 200- to 500-gate circuits, standardized on the basis of commonality among military systems requirements. The possibility of designing a set of standard circuits that meets the common requirements of a large enough number of military equipments to justify the initial investment remains to be examined. The overall cost reduction or performance improvements that might be effected in this way will depend on the number of different types of circuits required in relation to the fraction of standard MSICs that will finally be replaced. If a family of 50 or so military customized circuits could be identified, which would replace an appreciable fraction of the gates (perhaps 50 percent or more) of the standard MSICs in military systems and be compatible with the remainder, significant cost reductions or performance improvements could be achieved and all of the deterrents reduced or sidestepped.

The transition to the use of more highly integrated, commercially developed medium-speed bipolar circuits in military equipment has already begun (with the AN/UYK-30 and AYK-14, for example) and will undoubtedly continue; however, how soon and how thoroughly this process, if left to itself, would produce a family of circuits well-adapted to the common requirements of military digital processing equipment is a matter for conjecture.

4. Circuit Speed and Level of Integration

Most of the current military digital processing equipment uses MSICs with 20 to 50 gates that operate at clock frequencies of about 10 MHz. (See Section V and Ref. 16.) These include

general purpose computers,* radar and sonar signal processors, vocoders, communications encoders and decoders, etc. Schottky bipolar and LS TTL bit-slice devices of the same speed are being produced with a few hundred gates/chip, and I^2L devices such as a 16-bit microprocessor, with 4000 gates and 6-MHz clock are now offered. TRW offers special medium- and high-speed devices in 3D (triple diffusion) technology with a few thousand gates.** The 4000-gate PMOS and NMOS circuits now in production operate at maximum clock speeds of 1 to 3 MHz.

5. High-Speed ICs

The ECL ICs operate at 50 MHz-clock frequency, which approaches the present practical upper limit for digital circuitry (because of lead length, noise problems, etc.); but an ECL gate typically dissipates 20 mw which limits the level of integration to 100 gates/chip unless extraordinary measures are used to remove excess heat resulting in weight and cost penalties which offset much of the advantages of higher circuit integration.

6. I^2L, SFL, CMOS/SOS LSIC Technology

I^2L circuits will operate over the military temperature range (-55°C to 125°C), and it appears likely that software can be developed for the automatic design and layout of I^2L LSIC chips. Furthermore, the calculated throughput capacity per chip or per watt is higher for I^2L than for any other circuit technology except triple diffusion (3D) (see Table 2, p. 66).

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*Such as the UYK-7.

**"However, at (bipolar) performance levels, circuits with several thousand gates are not...practical for technical and economic reasons. Power dissipation is high and requires...cooling....the market for high performance circuits is fractured and limited....the designer of high performance digital systems cannot accept (MOS) LSI building blocks and...usually cannot afford...custom LSI...." (Reference 17.)

CMOS/SOS and silicon-gate CMOS are expected to become available as medium-speed technologies; they will be somewhat faster than I^2L but will not provide as high a level of integration. The development of efficient automatic design software for fully customized circuits is said to be simpler for I^2L than for any other established circuits technology.

7. Cost and Lead Time

In currently available LSIC technologies (3D, PMOS, NMOS, CMOS), the design and prototype development costs for a new 4000-gate chip range typically from $100K to $1M, with a lead time of six months to two years. The comparatively high cost and lead time for the development of MOS LSICs are due, in part, to the unavailability of automatic (computer) layout and design programs. (Computer design aids in the form of interactive graphics, operation simulation, tape-driven plotters and drafting machines, etc., are widely used.) New production techniques, such as electron beam lithography (Section VII) may eventually reduce the lead time for prototype development, while automatic computer design of the chip layout (from a logical design) would substantially reduce development cost and lead time.

8. Microprogrammable Bit Slice and Mask Programmable LSICs

An LSIC family of microprogrammable bit slices (Section VI-B) may eventually prove to be satisfactory for a substantial part of special military IC applications (such as signal processing). Bipolar bit slices and their controller are now available from several sources. When utilized with high-performance bipolar ROMs and PROMs, the microprogrammable bit slices offer more compact, reliable, and cheaper embodiments than standard MSICs. The bit-slice circuits typically contain several hundred gates and operate at 5 to 10 MHz microinstruction execution rates.*

*"Variable architecture (microprogrammable) processors are able to satisfy the high performance/speed applications which MOS processors fail to meet." (Reference 21.)

The microprogram can be changed by substituting ROM codes and the design can be modified and corrected in hours (Ref. 17).

The AN/UYK-30 microcomputer consists of commercially available, second-sourced microprogrammable bipolar bit slices, plus standard TTL MSICs, and exhibits improvements in physical qualities and unit cost consistent with the analytical models used in this study (Ref. 46).

If a satisfactory high-speed LSIC (a few thousand gates/circuit) technology emerges (such as I^2L, SFL, DMOS, CMOS on SOS), a mask programmable standard cell LSI approach might eliminate many principal objections to the use of custom LSICs in military systems, provided the device will not need to be requalified for each different interconnect metallization pattern.

9. Very Large Scale Integration (VLSI)

ICs with 10,000 or more gates could probably be fabricated using current production technology, and they would probably exhibit comparative cost, weight, power consumption and reliability benefits consistent with the formulas used in this paper. However, a net economic incentive for introducing VLICs in military systems probably would not exist except when the systems support costs were extraordinarily high, or a demand exists for tens of thousands of circuits, or the circuit received substantial production support from the commercial sector.

B. DOD LSIC PROGRAM OPTIONS

The following is a list of possible DoD measures for realizing the potential cost and performance benefits of more highly integrated circuits.

1. Initiate a program to develop a standardized military family of medium- (or higher) speed ICs with at least a few hundred gates/chip. The logical and physical design of the members of a family of military standardized circuits necessarily

involves a number of compromises relating to circuit technology, systems engineering, design and production costs, standardization and commonality, and so on, which must be based, in part, on background information about the foreseeable military procurements involving IC equipment.

A conservative approach would be to identify blocks of logical functions that do not violate the conditions of integrability, speed, compatibility, etc., and select a group which is generally applicable to military needs while relying on the standard MSI 54/74 series to fill the remaining gaps. Other things being equal, circuits that are likely to draw production support from the commercial sector are preferable since this would tend to lower their selling price and assure their continued availability. Microprogrammable (variable architecture) bit slices and mask programmable standard cell arrays should be included as candidates for evaluation.

A program of this kind, if successful, would produce the fullest benefits of circuit integration by:

a. distributing all of the nonrecurring costs over the largest number of military applications,
b. creating a large and sustained market to attract competitive bids from IC manufacturers, and
c. combining the economic benefits and superior physical characteristics of LSICs with the logistics advantages of standard circuits.

2. *Require systems project offices and weapons systems program managers to evaluate total LCCs of LSIC embodiments (including bit slices and custom circuits) as an alternative to the use of standard MSICs.* This would give the LSIC vs. standard MSIC choice higher visibility and would provide the weapons systems suppliers with incentive to bring IC manufacturers in at the systems development stage.

3. Consolidate purchases and mandate procurement policies that make the military digital equipment market directly accessible to the IC manufacturer. This would provide incentive for the fullest competition among IC manufacturers.

4. Institute interface and module standardization, use of federated power supply, etc., to facilitate retrofit and replacement. To put these possible measures in clearer perspective, they are elaborated and restated in the following tables. Table 7 lists IC device types in the order of their increasing speed, showing typical military uses and the applicable DoD policies and actions.

Table 8 lists the principal obstacles to the introduction of more highly integrated circuits in military applications, as well as relevant corrective measures.

TABLE 7. IC DEVICE TYPES

DEVICE TYPES	SPEED	MILITARY USES	DOD ACTION
MOS microprocessor, programmable read-only memories, random access memories, etc.	Low (1 - 3 MHz)	Embedded controllers, teletype terminals, etc.	Approve funding for military qualification program; standardize software
Microprogrammable (variable architecture) bit slices	Medium (5 - 10 MHz)	Probably widespread, but subject to determination	Determine applicability; require technical and LCC evaluation by weapons systems project offices, program managers
Standardized military IC family	Medium (10 MHz) to high (50 MHz)	Radar and sonar beam forming and signal processing, military computers, encoders and decoders, speech abstraction and synthesis	Study feasibility

TABLE 8. DETERRENTS AND POSSIBLE CORRECTIVE MEASURES

DETERRENT	POSSIBLE CORRECTIVE MEASURES
Schedule and cost risks in custom circuit development; large initial cost. LSI technology obsolesence	• Develop standardized military LSIC family to distribute cost and risk, and to simplify logistics • Encourage module standardization, use of federated power supply, etc., to facilitate replacement and retrofit • Consolidate purchases to generate large enough orders to keep technology alive, if necessary
IC manufacture application of engineering to maximize gross sales	• Consolidate purchases to attract competitive bids • Open equipment bids to semiconductor manufacturers
Risk avoidance by program managers, systems project offices	• Require LCC justification for use of standard MSICs rather than commercially available bit slices or military standardized LSICs
Future IC technology improvements and obsolescence of current technologies	• Design for retrofit

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APPENDIX A

A SIMPLE ANALYSIS OF DIRECT LIFE CYCLE COST OF INTEGRATED CIRCUIT ASSEMBLIES

APPENDIX A

A SIMPLE ANALYSIS OF DIRECT LIFE CYCLE COST OF INTEGRATED CIRCUIT ASSEMBLIES

Consider first an assembly of ICs grouped on identical modules (printed circuit boards with connectors). Let ZETA be the failure rate of an individual IC, including failures associated with connectors. (In fact, a major source of reliability improvement associated with higher levels of integration is the reduction in number of connectors/gate.) ZETA is 2.5×10^{-6} log (NGPC) by the RADC model (Ref. 19), NGPC being the number of gates on the IC.

The number of ICs in the entire assembly is the ratio of N (the total number of gates in the assembly) to NGPC, and the total failure rate, DR, of ICs in M deployed systems, each of which contains one IC assembly is

$$DR = \frac{M \times N \times ZETA}{NGPC} \quad .$$

If false fault determinations are considered, this formula becomes

$$DR = M \times N \times \left\{ \frac{ZETA}{NGPC} + \frac{FFR}{LFI} \right\} \quad ,$$

where FFR is the false fault rate and LFI is the level of fault isolation.

In order to avoid logistic delays which would render the weapons system inoperable, a number of spare modules must be kept on hand for immediate replacement of those which are found to contain a defective IC. This number of spare modules is pro-

portioned to DR and the mean time which elapses between the failure of a module and its replacement or its repair and return to stock at the operating base. Some fraction, B, of the failures will result in condemnation and discarding of the entire module and, over the total operational life, TL, of the equipment, will create a demand for B x DR x TL spare modules. The remaining failures can be repaired by isolating and replacing the failed IC and, if this can be done in some average interval, TAU, the additional average number of modules in the repair pipeline at any time will be (1-B) x DR x TAU.

The average time (TAU) that a failed module remains in the repair pipeline can be expressed in terms of the average repair delay, TAUB (B for base repair), when the module is repairable at the operating base (this will occur with some fraction ALPHA of the failures) and the mean repair delay, TAUD (D for depot repair), when the module must be returned to a depot. TAUD would include not only the repair time at the depot, but also shipping time and other considerations. It is the practice in the fleet, for example, to return the failed units which have been accumulated during a cruise to the depot when the ship returns to port. In that case, TAUD is actually twice the duration of a cruise provided the returned units can be repaired and returned to stores in a shorter interval than TAUD.

In general then,

$$TAU = ALPHA \times TAUB + (1 - ALPHA) \times TAUD \quad .$$

In a similar manner, the average cost of repair can be expressed in terms of ALPHA and the costs of repair at the base and at the depot. In either case, replacement ICs must be on hand; over the entire operating life of the equipment (TL), a total of (1-B) x DR x TL will be needed, on the average.

Then the average number of spare modules in the pipeline is

$$ANSM = DR \times [(1-B) \times TAU + B \times TL]$$

and the average number of spare ICs needed for the repairable modules would be

$$ANSIC = DR \times (1-B) \times TL \quad .$$

The total cost of the spare module and ICs (CS) in terms of the unit cost/circuit (UCPC) and the unit cost/module (UCPM) is

$$CS - ANSM \times UCPM + ANSIC \times UCPC \quad ;$$

but in terms of the number of gates/module (NGPM), and number of gates/circuit (NGPC),

$$UCPB = \left[\frac{NGPM}{NGPC} \times UCPC + CB\right] \quad ,$$

where CB is cost of the board itself.

We designate by CF the ratio $\frac{NGPM}{NGPC}$ and note that CF can be no less than unity; then

$$UCPM = (CF \times UCPC + CB) \text{ and}$$
$$CS = ANSIC \times UCPC + ANSM \times (CF \times UCPC + CB) \quad .$$

The cost of repairing or replacing, CR, failed boards is proportional to the total number of failures over the life of the system DR x TL and will depend on the cost of repair (RA) for the fraction (1-B) or repairable failures, and the cost of replacement (RE) in the remaining cases as follows:

$$CR - DR \times TL \times [(1-B) \times RA + B \times RE] \quad .$$

The acquisition cost on the other hand is

$$CA = \frac{UCPC \times M \times N}{NGPC} \quad , \text{ in terms of which}$$

$$CS = A \times ZETA \times TL \times \left\{(1-B) + [(1-B) \times \frac{TAU}{TL} + B] \times \left(CF + \frac{CB}{UCPC}\right)\right\}.$$

The sum of these costs divided by the total number (N x M) of gates in all systems gives the total of the direct life cycle components of cost (per gate):

$$CT = \frac{(CA + CS + CR)}{N \times M} .$$

The economic benefits of higher levels of integration can be seen through the coefficient $\frac{UCPC}{NGPC}$ and in ZETA. At higher levels of integration, both of these quantities diminish. Historically, this has been the case for increases in the level of integration from one to several thousand and can be expected to be so for future increases in circuit integration to several tens of thousands of gates/IC (Ref. 6).

In Fig. 8, p. 38, CA, CS and CR are plotted for the following set of parameter values:

LFI (= NGPM)	: 3,000 gates
TL	: 20,000 hours
B	: 0.05
ZETA	: $2.5 \times 10^{-6} \ LOG_{10} \ (NGPM)$
UCPC	: $\$9.60 \ (NGPC)^{0.38}$
RA	: \$200
RE	: \$50
TAU	: 1000 hours

APPENDIX B

CIRCUIT CHARACTERISTICS OF THE PRINCIPAL LSIC TYPES

APPENDIX B

CIRCUIT CHARACTERISTICS OF THE PRINCIPAL LSIC TYPES

In the following pages, some of the most important logic families are described briefly and representative characteristics are listed. Some families, such as Diode Transistor Logic (DTL) and Resistor Transistor Logic (RTL), appear to be obsolescent at present and have been omitted. Others, such as VMOS, DMOS and SFL, appear to be promising but are not in commercial use at this time, and are, therefore, omitted.

1. Device: TTL Bipolar "Transistor-Transistor Logic"

Structure: A multi-emitter bipolar transistor is arranged to drive a single output terminal through a bipolar transistor inverter (Figs. B-1 and B-2).

Process: 7 masks, 4 diffusions.

Density: 50 mil^2/gate (30 gates/mm^2).

Level of Integration: 50-100 gates.

Gate Delay: 6-14 nsec; typical clock speed of 5 MHz.

Power-Delay Product: 100 pj.

Power/Gate: 10 mw (internal); 15 mw (off chip).

Fan-Out Capability: 1-10 at all clock frequencies.

Circuit Characteristics: Fast, low impedance, good driver for interconnection conductors. Low impedance input. Output impedance typically less than 100 ohms.

Noise Immunity: 20 percent of supply voltage.

Supply Voltage: 3-30 volts, 5 volts typical.

External Factors: In widespread use; other devices are preferably "TTL compatible." Commonly used to drive large capacitance connecting conductors to other chips or devices. Test load for output: 400Ω and 15 pf.

Input Capacitance: 0.8 pf/gate input, typical.

Input Resistance: 400 ohm, typical.

Disadvantages: Large power requirements relative to MOS. Low input impedance requires substantial driving power.

Cost: TTL is slightly more costly than most MOSFET circuits, but its performance characteristics, especially its speed, power output and the ability of one TTL gate to drive up to 10 similar gates, has made it widely used at present.

Comments: TTL evolved from an older system in which a transistor was driven by an array of diodes, termed "Diode-Transistor Logic," or DTL. TTL Logic is now so widely used that other IC families are specified "TTL compatible" when possible as a step toward standardization.

As compared with MOS families of LSI, TTL is faster but uses much more power/gate, so that care is necessary in chip design with TTL to avoid overheating.

As compared with emitter-coupled logic, TTL is slower but requires less care in layout and interconnection design, since the extreme speed of ECL, together with its high gate input impedance, tends to cause ringing and/or parasitic oscillations. Prevention of these troubles with ECL requires the addition of other circuit elements, such as line termination resistors, adding cost and complexity as compared with TTL.

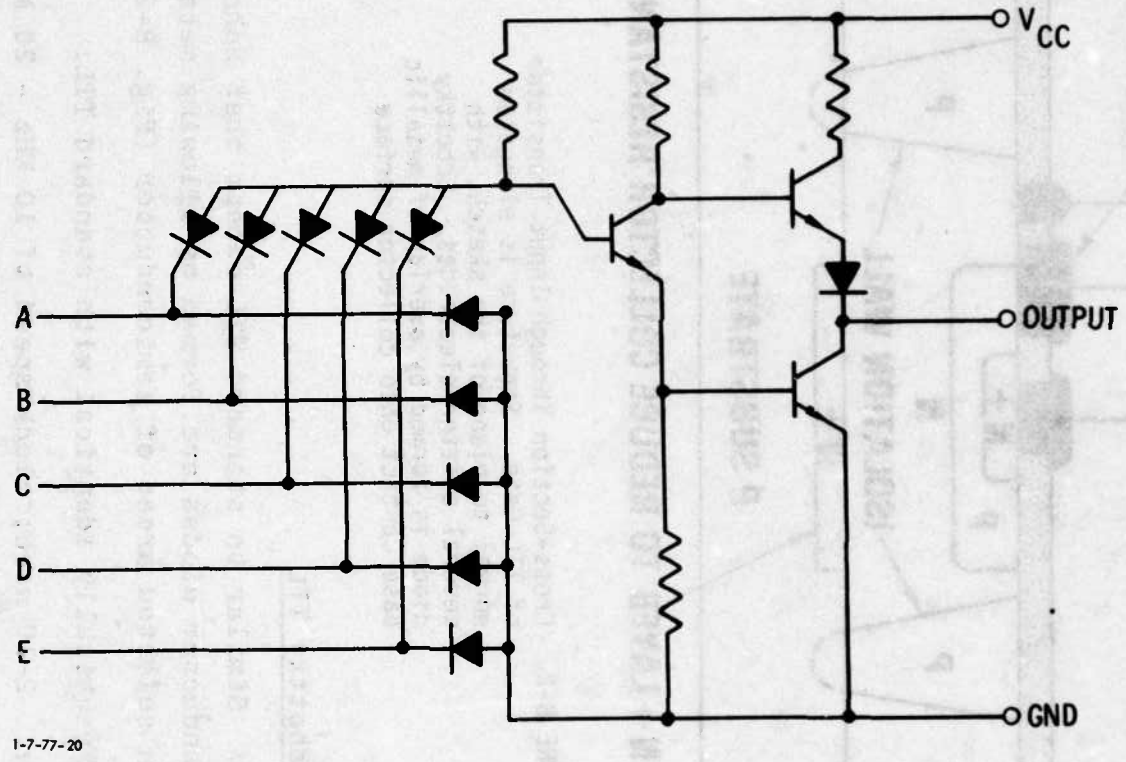

FIGURE B-1. TTL Positive NAND Gate and Inverter with Totem Pole Output

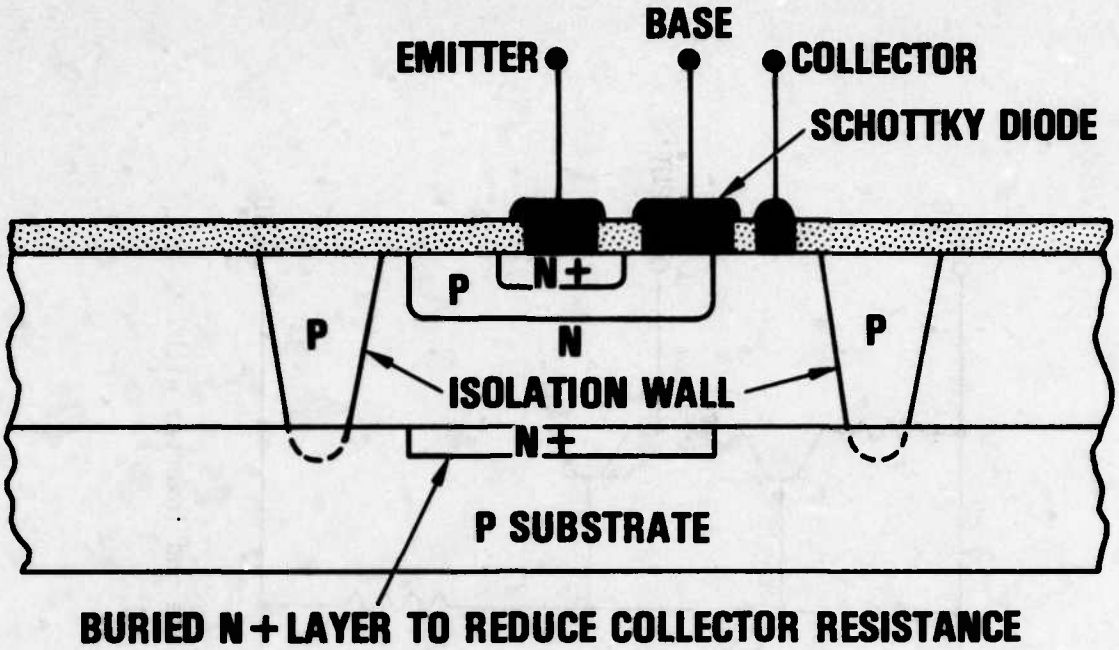

FIGURE B-2. Cross-Section Through Input Transistor of TTL Gate. Structure is elongated normal to plane of the sketch, with several emitter electrodes. Schottky diode is formed by overlap of metallic base contact onto collector surface

2. Device: Schottky TTL

Structure: Similar to standard TTL except that Schottky metal-to-semiconductor diodes are formed by allowing metal to be deposited on selected areas of semiconductor (Fig. B-2).

Process: Practically identical with standard TTL.

Gate Delay: 2-10 nsec; clock speed of 10 MHz - 20 MHz.

Density: 20 mil^2/gate.

Level of Integration: 300 gates/chip.

Power-Delay Product: 10 pj.

Power/Gate: 5 mw (internal).

Fan-Out Capability: 1-10.

Circuit Characteristics: Similar to TTL but faster (Fig B-3).

Noise Immunity: Same as standard TTL.

Supply Voltage: Same as TTL, typically 5 volts.

External Factors: Similar to standard TTL except low-power versions of Schottky TTL can achieve higher levels of integration, i.e., 500 gates/chip.

Input Capacitance: Similar to standard TTL.

Input Resistance: Similar to standard TTL.

Disadvantages: Similar to standard TTL.

Cost: Similar to standard TTL.

Comments: Speed of basic TTL gate was notably improved by a slight modification of the manufacturing process, which caused the metallic contact to the transistor-base electrode to overlap the collector semiconductor surface to form a metal-to-semiconductor "Schottky" diode between base and collector. Such a diode conducts by majority carriers and prevents the collector from falling to so low a potential that it "saturates" or fails to collect minority carriers from the base. As a result, the collector can rise in potential rapidly at the end of a current pulse without the necessity to mop up a dense cloud of minority carriers, which considerably increases switching speed as compared with standard TTL.

A low-power version of Schottky TTL exists that dissipates only 2 mw/gate while maintaining a switching speed of 9.5 nsec.

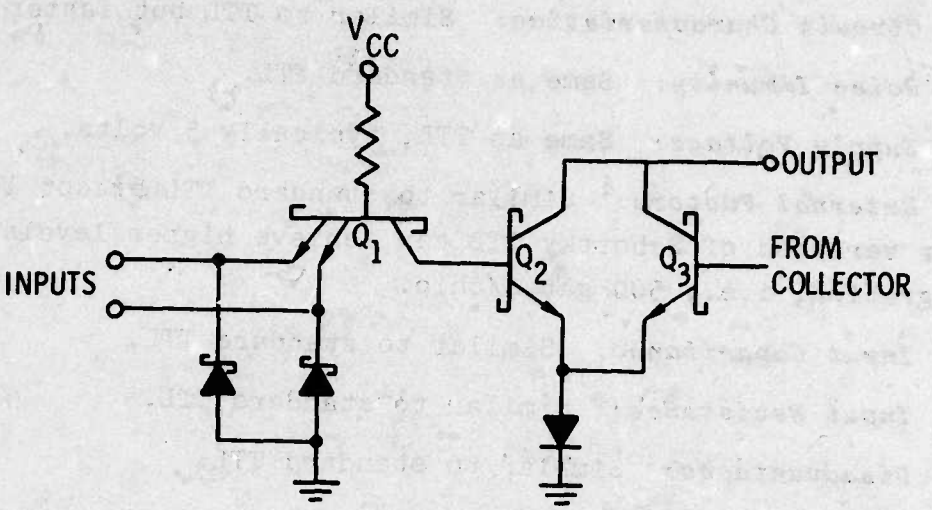

FIGURE B-3a. Schottky MSI Circuit

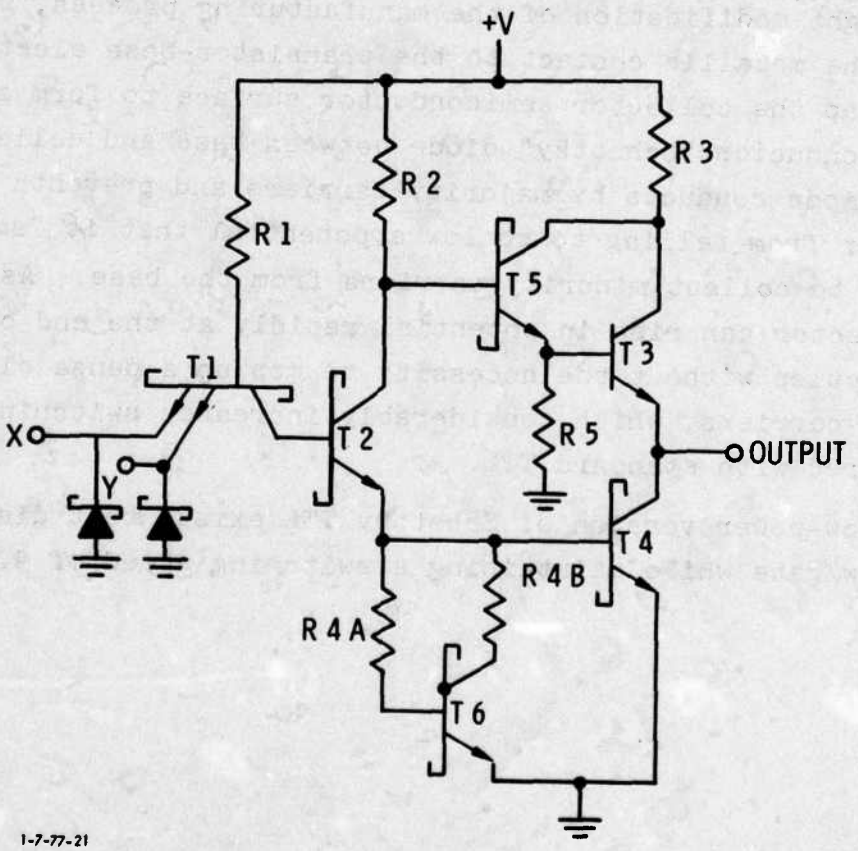

FIGURE B-3b. Schottky Clamped TTL Logic Gate with Totem Pole Output

3. Device: PMOS "P-Channel, Metal Oxide-Semiconductor"-Field-Effect Transistor

Process: 4 masks, 1 diffusion.

Structure: On an N-type substrate, two closely spaced coplanar P-type electrodes, called the "source" and the "drain," are formed by diffusion. The narrow strip of semiconductor surface between the two electrodes is covered with insulating oxide on which is deposited a metal "gate" electrode. Negative potential on the gate causes minority charge carriers (holes) to invade the semiconductor surface under the gate, forming a conducting bridge between source and drain. The conductivity of this bridge is modulated by variations of gate potential.

Density: 150 gates/mm^2 (10 mil^2/gate).

Level of Integration: 4000 gates/chip.

Power-Delay Product: 200 pj.

Power/Gate: 2 mw (internal).

Delay Time: Typically 100 nsec/gate, clock speed 800 kc.

Fan-Out Capability: Typically 3; delay time increases with fan-out; large DC fan-out capability.

Noise Immunity: 30 percent of supply voltage.

Supply Voltage: Typically -10 volts; +5 volt bias supply.

Circuit Characteristics: Low-power consumption, extremely high input impedance; slower than most bipolar logic; output impedance high in "off" condition, 2000 ohms in "on" condition.

External Factors: TTL compatible.

Input Capacitance: 0.5 pf/gate.

Input Resistance: 10^{12} ohm.

Disadvantages: Slow compared with NMOS or most bipolar logic. Two supply voltages required.

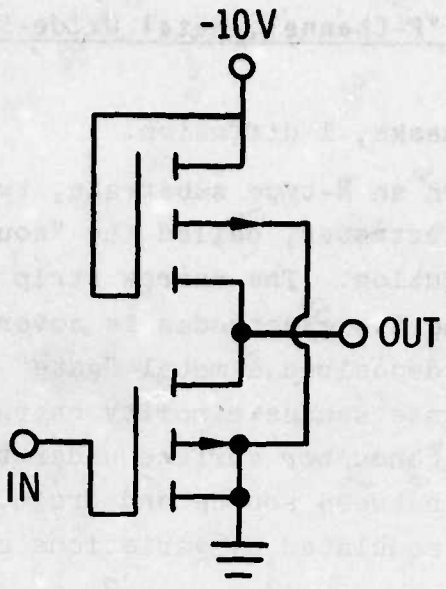

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FIGURE B-4. Basic PMOS Inverter

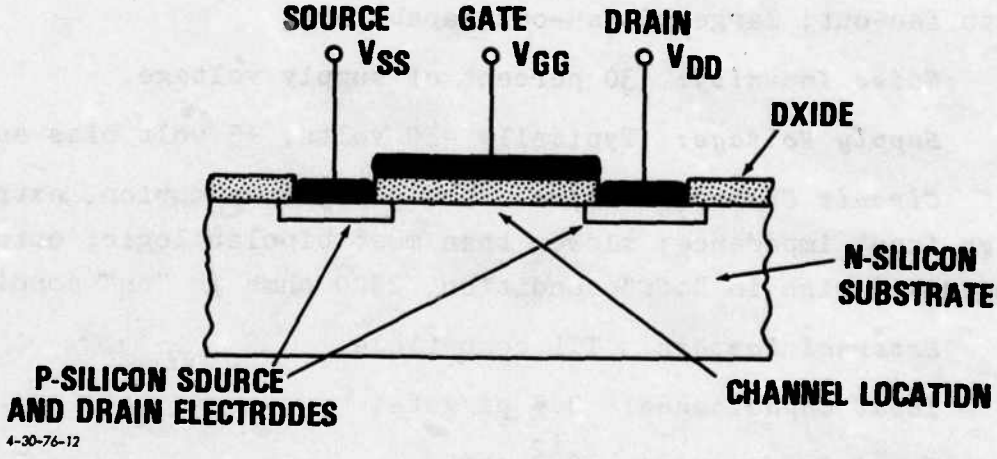

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FIGURE B-5. PMOS Structure

Cost: Lowest cost of any IC technology.

Comments: The PMOS field-effect transistor was the first form of MOSFET to be extensively utilized for ICs and still is the least expensive. It features low-power consumption, extremely high input impedance, and high density. Ordinarily, no isolation walls are required because neighboring devices are effectively shielded from each other by the conducting substrate which serves as a ground plane. PMOS devices ordinarily do not conduct until the gate electrode is made more negative than a definite threshold bias, so that they are said to operate in the "enhancement mode," conductivity being enhanced by the gate potential.

Unfortunately, most applications require a bias voltage supply in addition to the output circuit power supply, adding slightly to the circuit complexity. PMOS devices with constant gate potential can serve as resistors with some resultant manufacturing simplification.

The small current output that characterizes PMOS (and other MOSFET transistors) results in slower gate action than can be readily obtained with bipolar transistors, a disadvantage somewhat offset by manufacturing simplicity, low-power consumption, and high density.

4. Device: NMOS "N-Channel Metal-Oxide Semiconductor"-Field-Effect Transistor

Structure: On a P-type silicon substrate, an N-type source and a drain electrode are formed by diffusion, separated by a short space covered by a gate electrode. Positive voltage augments conduction between source and drain by electrons in the surface space charge layer of the substrate while negative voltage on the gate tends to reduce conduction. If the gate electrode is formed of metal deposited on SiO_2, conduction exists between source and drain with zero potential difference

between gate and substrate, a negative bias being required to cut off conduction. Commonly, the gate electrode is specially processed to eliminate this zero-bias conduction, causing the device to operate in the enhancement mode as does PMOS.

Process: 4 masks, 1 diffusion.

Density: 200 gates/mm^2 (6 mil^2/gate).

Level of Integration: 4000 gates/chip.

Power-Delay Product: 20 pj; approaches 40 pj for silicon gate version.

Power/Gate: 5 mw.

Delay Time: Typically 30 nsec (lower at higher supply voltages); clock speed 3 MHz.

Fan-Out Capability: Generally same as PMOS, typically 3, capable of very large fan-out at low frequencies.

Noise Immunity: Similar to PMOS except low threshold voltage reduces noise immunity in some circuits.

Supply Voltage: Typically +5 and +12 volts, both required.

Circuit Characteristics: Low-power consumption; extremely high input impedance; slower than most bipolar logic; output impedance typically 2000-4000 ohms. Can operate in depletion mode or enhancement mode, depending on processing. Substantially faster than PMOS.

External Factors: Similar to PMOS but faster; TTL compatible.

Input Capacitance: 0.5 pf/gate.

Input Resistance: 10^{12} ohm.

Disadvantages: More complex process than PMOS: special treatment required to avoid formation of overall N-channel near surface. Tends to operate in depletion mode unless specially

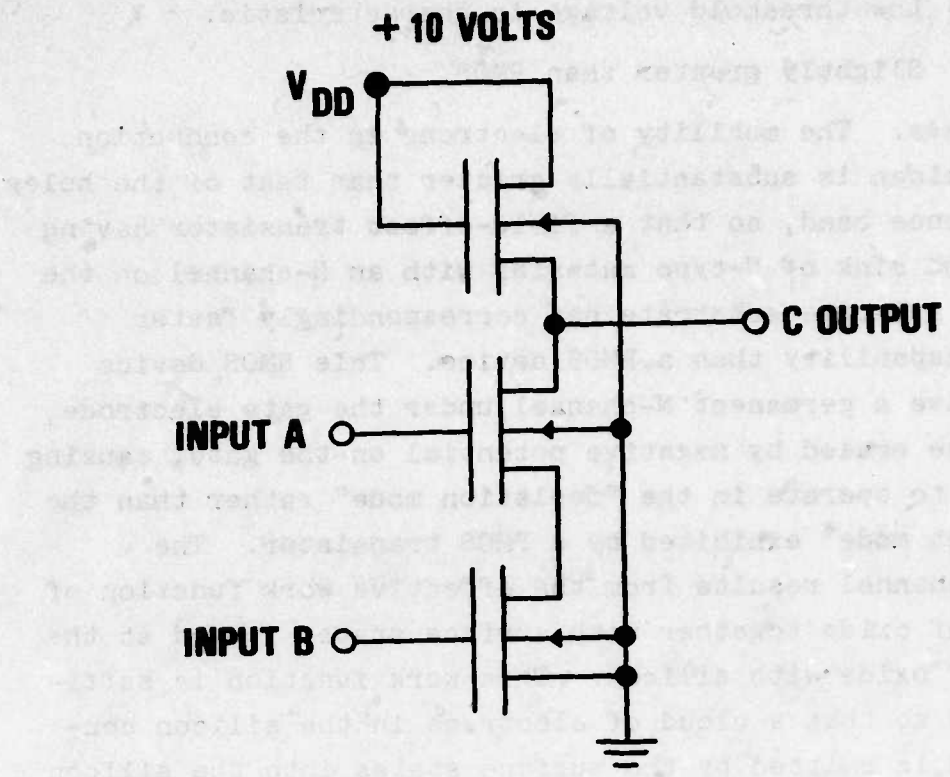

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FIGURE B-6a. NMOS NAND Gate (Enhancement Mode)

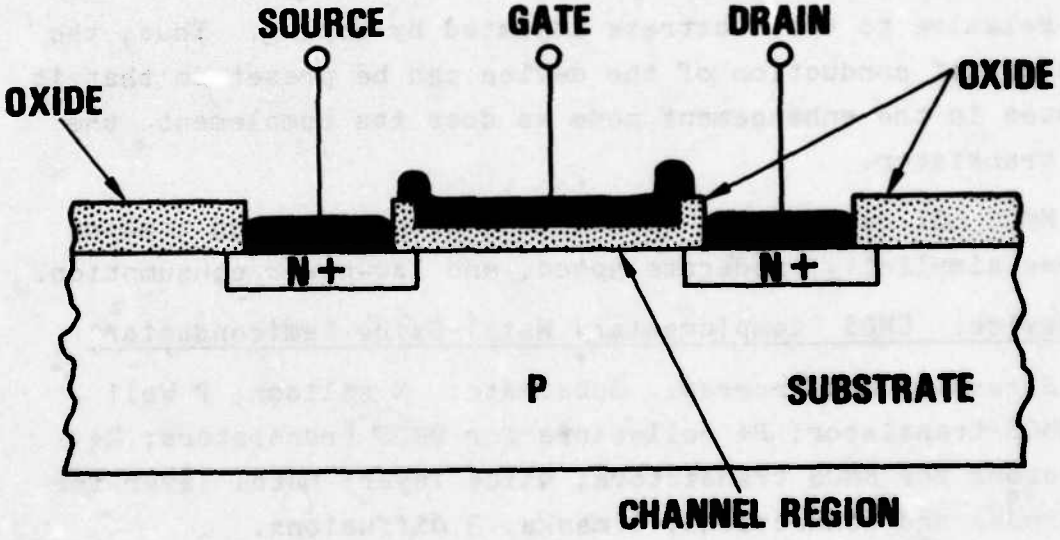

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FIGURE B-6b. MOS Structure

processed. Low threshold voltage is characteristic.

Cost: Slightly greater than PMOS.

Comments: The mobility of electrons in the conduction band of silicon is substantially greater than that of the holes in the valence band, so that a field-effect transistor having a source and sink of N-type material with an N-channel on the surface of a P-type substrate has correspondingly faster switching capability than a PMOS device. This NMOS device tends to have a permanent N-channel under the gate electrode, which can be erased by negative potential on the gate, causing the device to operate in the "depletion mode" rather than the "enhancement mode" exhibited by a PMOS transistor. The permanent channel results from the effective work function of the layer of oxide together with surface states formed at the junction of oxide with silicon. This work function is sufficiently low so that a cloud of electrons in the silicon conduction band is emitted by the surface states into the silicon surface. The work function can readily be modified by changing the nature of the oxide film, or more commonly, by replacing it with polycrystalline silicon which can have its work function relative to the substrate adjusted by doping. Thus, the threshold of conduction of the device can be preset so that it operates in the enhancement mode as does its complement, the PMOS transistor.

NMOS LSI devices are widely used at present and combine process simplicity, moderate speed, and low-power consumption.

5. Device: CMOS "Complementary Metal-Oxide-Semiconductor"

Structure and Process: Substrate: N silicon; P Well for NMOS transistor; P+ collectors for PMOS transistors; N+ collectors for NMOS transistors; oxide layer; metal layer for electrodes and connections; 6 masks, 3 diffusions.

Density: 40 gates/mm^2 (50 mil^2/gate).

Level of Integration: 1000 gates/chip.

Power-Delay Product: 10 pj.

Power/Gate: 0.5 mw.

Delay Time: 50-150 nsec at 3 volts; 15-45 nsec at 10 volts (3 MHz clock).

Fan-Out Capability: Typically 3, depends on speed, DC fan-out capability 50.

Noise Immunity: 45 percent of supply voltage.

Supply Voltage: 3-10 volts, unregulated; typically 5 volts.

Power Requirements: Quiescent: 0.003 µw at 3 volts; 1 MHz clock: 70 µw at 3 volts; 780 µw at 10 volts.

Circuit Characteristics: Extremely low-power consumption in quiescent state; power drawn only during gating transitions; power drain increases with clock frequency directly. Slower than most bipolar logic. Extremely high input impedance. Output impedance typically 2000 ohms, 500 ohms for special line driver types.

External Factors: TTL compatible; thresholds: NMOS 0.8 to 1.2 volts; PMOS 1.3 to 1.7 volts.

Input Capacitance: 0.5 pf typical.

Input Resistance: 10^{12} ohm typical.

Disadvantages: Process complexity; slower than TTL; high impedance output; low power output. Requires subsequent buffer in many applications. Large area/gate as compared with NMOS limits level of integration.

Comments: Based on the use of both NMOS and PMOS transistors in complementary pairs, CMOS provides a great deal of design flexibility and some unique features at the cost of

added manufacturing complexity and slightly larger area/active element than other MOS structures.

The speed of CMOS gates is greater than that of other conventional MOS gates, and it switches near the center of the range from high- to low-output potential, providing a noise immunity of 45 percent of the supply voltage.

It is the low-power consumption of CMOS that is its unique characteristic. The input resistance of a gate in a quiescent state, either at the high- or low-switching potential, is in excess of 10^{12} ohms. A CMOS gate can be so designed that the two transistors comprising the basic gate never conduct simultaneously when the input is at ground potential; the upper PMOS transistor conducts, connecting the output to the 5-volt supply; when the input is at 5+ volts, the NMOS transistor conducts, connecting the output to ground. The two transistors normally do not ever conduct simultaneously so that power consumption results from charging and discharging the output capacitance once/clock cycle. For example, if the output capacitance is 15 pf, the power supply voltage is 5 volts and the clock frequency 3 MHz, then the power drain on the 5-volt supply is:

$$\begin{aligned} W &= \tfrac{1}{2} f C V^2 \\ &= 3 \times 10^{6} \quad \tfrac{1}{2} \quad 15 \times 10^{-12} \quad 25 \\ &= 563 \ \mu w \quad . \end{aligned}$$

For intra-chip circuitry, capacitance is usually less than 2 pf, so that power drain/gate is typically 110 μw for on-chip logic. Note that this power drain/gate varies directly with the clock frequency, so that slow systems such as process controls and some instrument controls can be designed with CMOS to have extremely small power consumption, such as 5 mw/1000 gates.

Figure B-7 illustrates the application of the basic CMOS gate to a typical logic structure, a positive NOR gate. Note that no resistors are required, and that a single power supply voltage is used.

Figure B-8 shows a cross-section of a CMOS basic gate. The clear areas are all single crystal silicon, with conductivity types as labelled formed by mask-defined diffusion of impurities into the original N-type slab. The stippled areas are silicon dioxide dielectric, and the dark areas metal, applied by vacuum evaporation.

6. Device: ECL "Emitter-Coupled Logic"-Bipolar Transistor

Structure: Emitter-Coupled Logic LSI gates make use of elongated multibase, common emitter, bipolar transistors. The elongated emitter consists of an N-type silicon formed by diffusion of phosphorous or arsenic into a P-type substrate. A buried N+ layer is usually located under the emitter to reduce its longitudinal resistance. The multiple-base electrodes are formed by diffusing a P-type impurity into the emitter, and collectors are formed by similarly diffusing an N-type impurity into the bases. One additional output transistor, plus two or three resistors, are required to comprise a typical ECL gate such as those shown in Fig. B-9.

Process: 6 masks, 5 diffusions, N+ buried layer, 1 epitaxial growth.

Density: 20-50 gates/mm^2 (30 mil^2/gate).

Level of Integration: 100 gates/chip.

Power-Delay Product: 15 to 65 pj (0-10 fan-out).

Delay Time: 1 nsec (0-10 fan-out), 50 MHz clock.

Fan-Out Capability: Large, typically 10.

Noise Immunity: Fair, due to low impedance output.

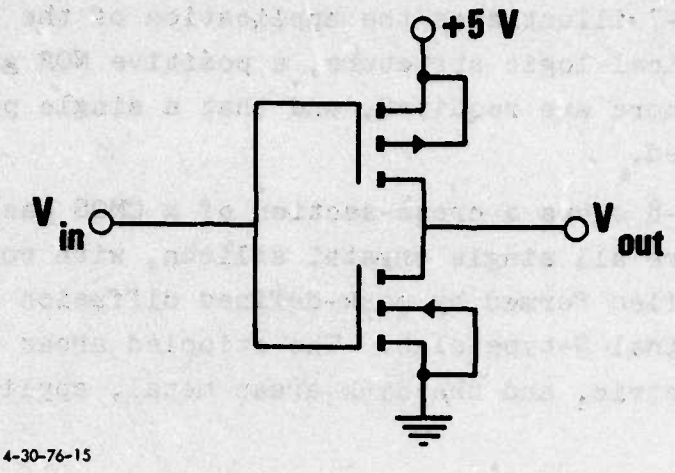

FIGURE B-7a. Basic CMOS Gate

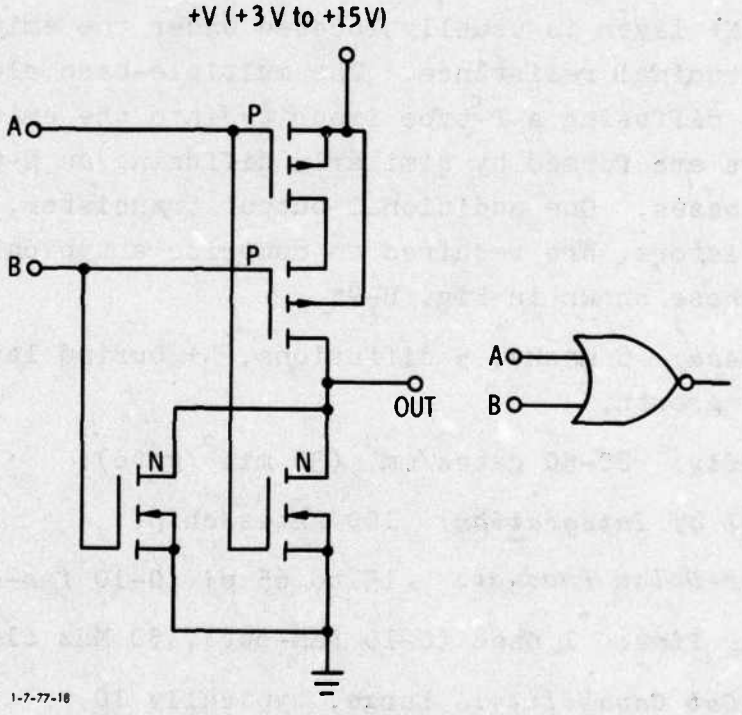

FIGURE B-7b. CMOS NOR Gate

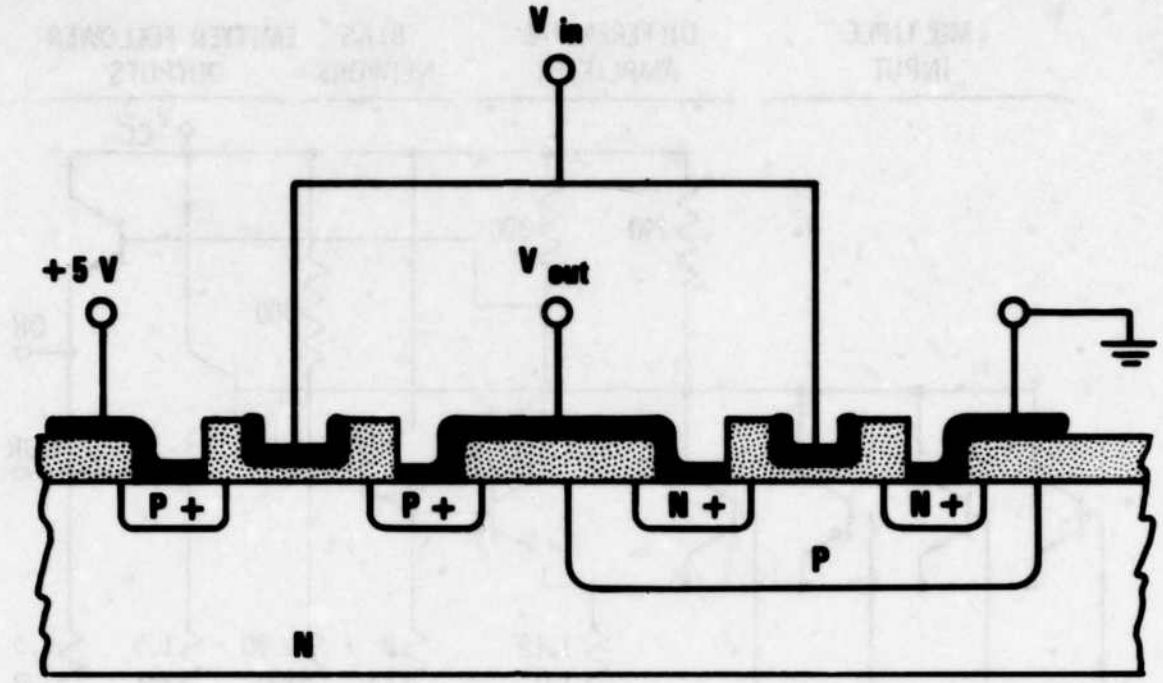

FIGURE B-8. CMOS Structure

Supply Voltage: 2-15 volts, 5 volts typical.

Power Requirements: 20 mw/gate (internal).

Circuit Characteristics: Nonsaturating; very fast; low impedance output, high impedance input. Requires careful design of interconnecting leads to prevent ringing. Can radiate interfering signals from fast transitions.

External Factors: Relatively large power output and dissipation, TTL compatible.

Input Capacitance: 1×10^{-12} F typical.

Input Resistance: 10^{4} ohm.

Disadvantages: Requires resistors; large power drain and dissipation/gate compared to MOS. High speed requires care in design and application to avoid ringing and parasitic oscillation. Awkward signal voltage levels, voltage swing of a fraction of a volt.

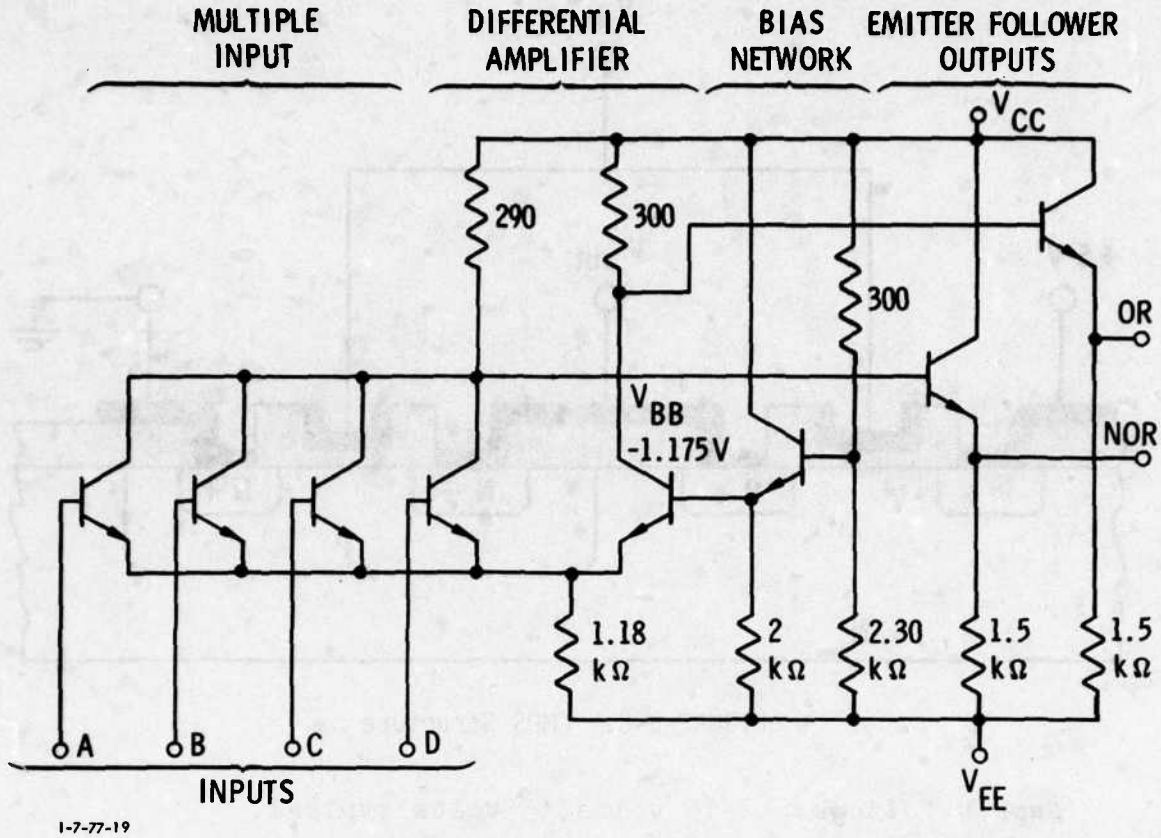

FIGURE B-9. Four-Input ECL Gate

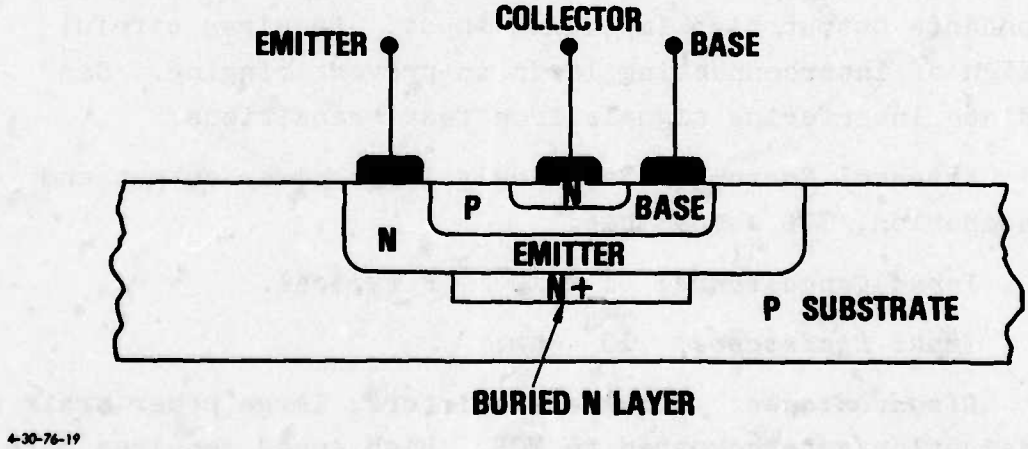

FIGURE B-10. Section Through ECL Common Emitter Transistor

Cost/Chip: Relatively costly.

Comments: ECL devices are noted for their very high switching speed (1-3 nsec) and high power and gain. At no point in their switching cycle do the circuits of an ECL system saturate so that no minority carriers are stored in any base which would delay switch action.

ECL is now the logic family most favored for large computer system application, mainly because of its high speed and relatively large fan-out capability.

The high gain, high speed, and high-input impedance of an ECL gate make it necessary to provide resistive terminations to interconnection lines to prevent ringing and/or unwanted high frequency parasitic oscillations. Power consumption is large compared to other forms of gates, and therefore, there are practical limits to the number of gates/chip and the necessity to provide for adequate heat dissipation. ECL would require further miniaturization to be usable as a logic family for LSI, but a few ECL gates could be used on an LSI chip using another family, such as I^2L, to provide fast input and output or multiplexing functions.

7. Device: I^2L "Integrated Injection Logic"-Also Known as MTL "Merged Transistor Logic"--Bipolar Transistors

Structure: An N-type emitter with an underlying N+ layer serves as the substrate for all transistor elements. P-type base elements, each with a plurality of collectors, are placed closely adjacent to a P-type constant-current injection electrode which injects a current of holes through the N-type substrate into the P-type base electrode, providing a current bias and making a load resistor unnecessary. The collectors may each be directly connected to the base electrodes of other similar transistors (Fig. B-11). A variation, substrate-fed logic (SFL), utilizes a buried P-layer as a current bias source instead of a laterally displaced electrode.

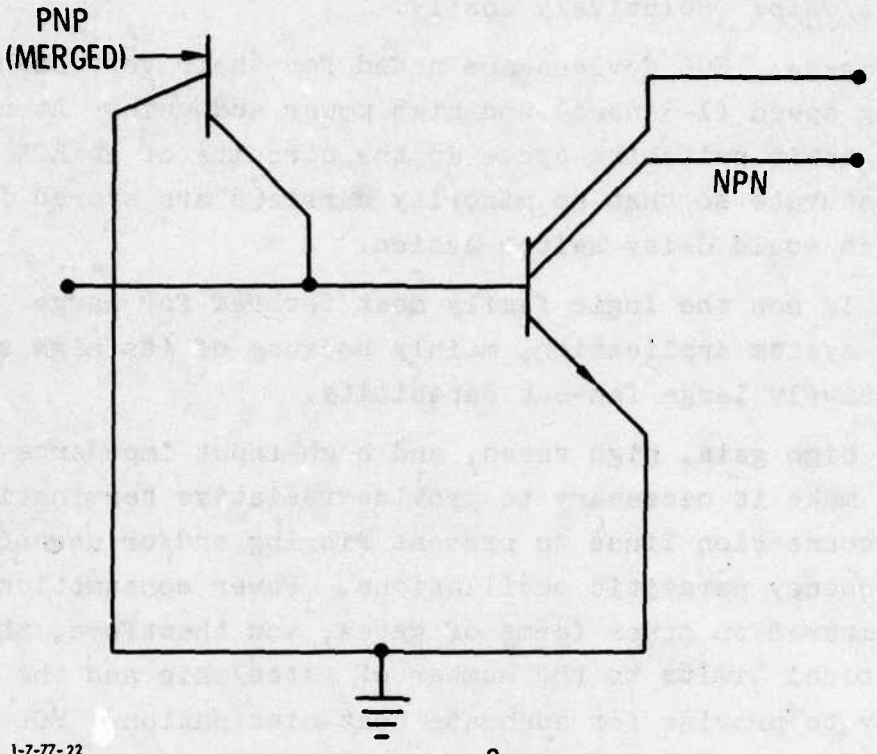

FIGURE B-11. Basic I^2L Inverter

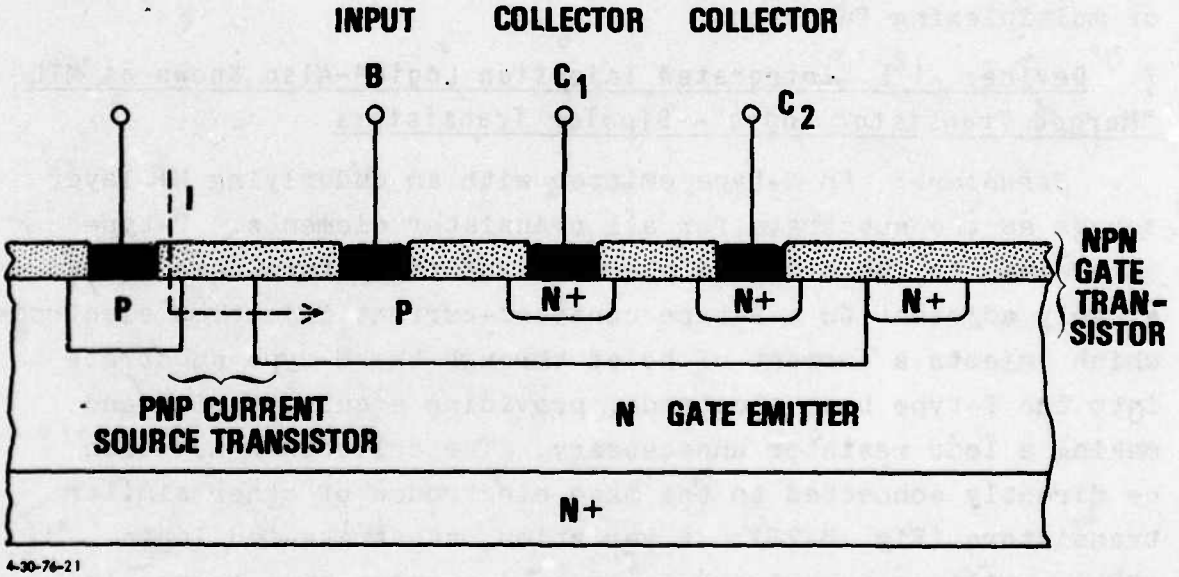

FIGURE B-12. Cross-Section of I^2L Structure

Process: 1 epitaxial growth, 2 diffusions, 4 masks.

Density: 300 gates/mm^2.

Power-Delay Product: 0.2-4 pj.

Power/Gate: 0.2 mw.

Delay Time: 10-30 nsec/gate, clock 10 MHz.

Circuit Characteristics: Low-impedance input, 1 μa - 1 ma current/transistor.

Fan-Out Capability: Typically 3; limited by available current.

Noise Immunity: Low impedance favors, while low-power supply lowers, noise immunity. Generally poor.

Supply Voltage: Low, usually 0.75 - 3 volts.

External Characteristics: Requires buffer, typically TTL, to drive other components.

Input Capacitance: 1.3 pf.

Output Capacitance: 0.3 pf.

Defects and Deficiencies: Low power level operation causes noise vulnerability; very low supply voltage somewhat inconvenient; low power output requires amplification to interconnect with other components. Not yet widely used.

Comments: Combining high density, automatic device isolation by the conducting common emitter, simplicity of manufacture, low power and high speed, the I^2L devices seem to be the most promising form of bipolar LSI yet developed. Each gate operates typically with only 1.5-volt power supply potential and produces an output voltage swing of only 0.6 volt, usually necessitating a modified transistor to drive interconnecting lines to other chips or devices.

The low intra-chip voltage levels tend to cause the I^2L

devices to be susceptible to electrical interference, although the low impedance level of the gates helps to ameliorate this. I^2L is only now beginning to be used for LSI on a large scale, and it is likely to occupy an important technological niche in the future.

APPENDIX C

FEASIBILITY OF LSICs WITH CLOCK SPEEDS GREATER THAN 10 MEGAHERTZ

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FEASIBILITY OF LSICs WITH CLOCK SPEEDS GREATER THAN 10 MEGAHERTZ

This study has found that ICs above the 1000-gates/chip level are not at present available to operate at the speed needed in many important DoD requirements. The study also finds that there is very high probability that these high-speed LSICs can be developed in the near future if a determined effort were directed to that objective. Below is a summary of the reasoning behind this finding.

A study of scaling of both bipolar and field-effect transistor circuits shows that circuit speed varies inversely with scale; that is, the smaller the linear dimensions of an IC, the higher the speed. Miniaturization increases the number of gates/chip as the inverse square of the linear dimensions, while the power dissipated/unit area remains constant, or, in the case of bipolar transistors, actually decreases with correctly scaled miniaturization.

Miniaturization requires further improvement of the resolution of the circuit structure-defining process, presently based on optical lithography. However, several laboratories are now developing E-beam lithography which can be used in at least three ways: (a) the electron beam can write directly on the photoresist on the surface of a ship; (b) it can be used to manufacture masks for optical contact printing which have much higher resolution than masks in current use; or (c) it can be used to produce mask patterns on photoemission cathodes.

All of these E-beam techniques appear to provide the necessary means to achieve the further miniaturization needed to meet DoD's LSIC requirements.

Combining the foregoing observations, it seems very likely that the application of E-beam techniques to produce correctly scaled miniaturization of one or more of the most promising logic families will be able to meet DoD high-speed LSIC requirements.

Further study of this prospect should determine the degree of miniaturization needed and to identify more specifically the most promising logic families for its application.

APPENDIX D

THE LIMITING SIZE OF BIPOLAR AND MOS TRANSISTORS

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THE LIMITING SIZE OF BIPOLAR AND MOS TRANSISTORS

It is possible to foresee the approximate limits to miniaturization of both bipolar and field-effect transistors. This technical note estimates these limits for planar structures fabricated on monolithic silicon.

B. Hoeneisen and C. A. Mead have explored the limitations to miniaturization of planar transistors (Ref. 43). These limitations are derived from the fact that the thickness of the carrier-free "depletion zones" in NP junctions cannot be reduced too far without the onset of avalanche breakdown in the materials of the transistors due to the very large electric field existing in such zones.

A general discussion of physical limits in digital electronics is contained in Ref. 35, which summarizes the results of Ref. 43 and many others. Especially pertinent are Figs. D-1a and D-1b (Ref. 35, Figs. 25A and 25B, respectively) which exhibit the minimum depletion zone width in planar bipolar transistors and the minimum allowable source-drain spacing for planar field-effect transistors.

From Ref. 35 is also available an empirical formula for the breakdown field, E_B, in silicon vs. doping density:

$E_B = 5.6\ N^{0.3}$ volts/cm, where N is the number of doping impurity atoms/cm^3.

Another important relationship is that expressing the depletion zone width of an abrupt NP junction between one lightly doped and one heavily doped portions of a crystal:

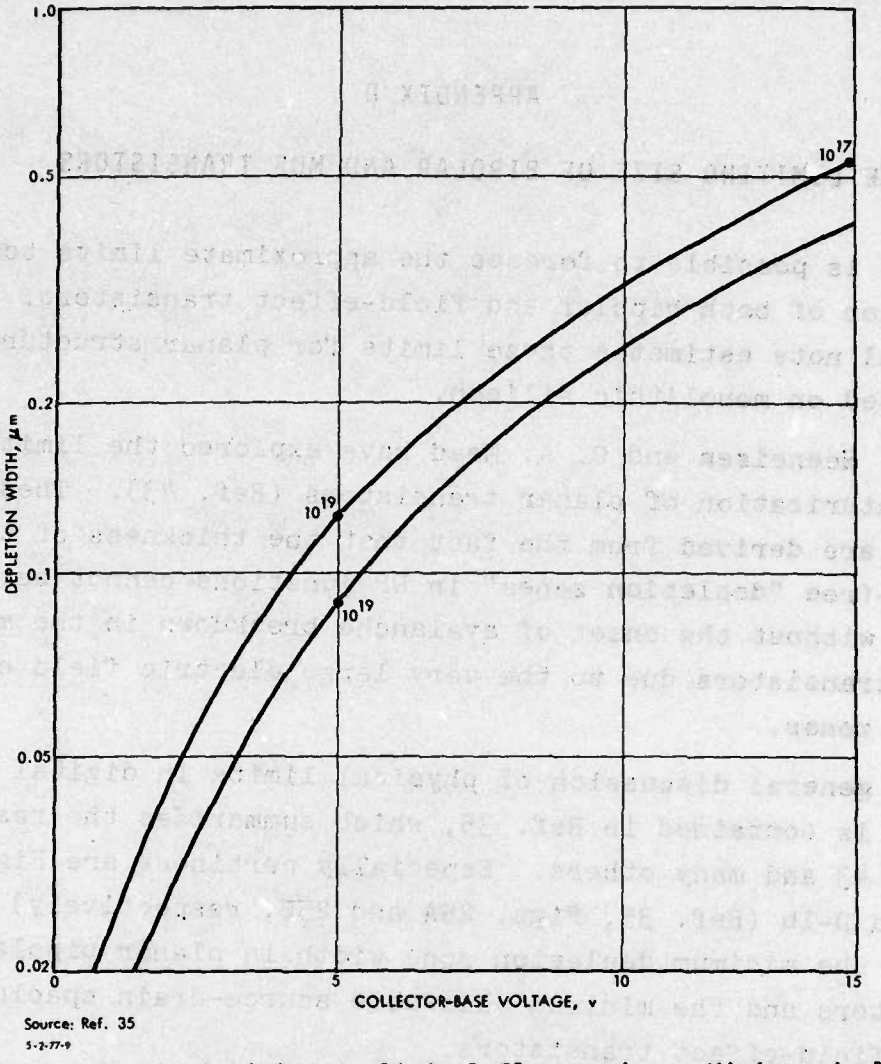

FIGURE D-1a. Physical Limits in Digital Electronics. Minimum depletion width of "isoplanar" bipolar transistor, in which base region is lightly doped with respect to emitter and collector, and diffused bipolar transistor, set by junction breakdown and punchthrough [after Hoeneisen and Mead (43)]. Doping levels are indicated

$$w = \sqrt{2\varepsilon(V + V_G)/Nq} \quad ,$$

where V_G is the forbidden bandwidth expressed in volts, the thickness w is in centimeters when ε, the dielectic constant of silicon, is 10^{-12} farad/cm, V is in volts, N is in atoms/cm^3 and q is the electronic charge, 1.6×10^{-19} coulomb.

In the following, the approximate number of logic gates/mm^2 is estimated on the assumption that an average of five

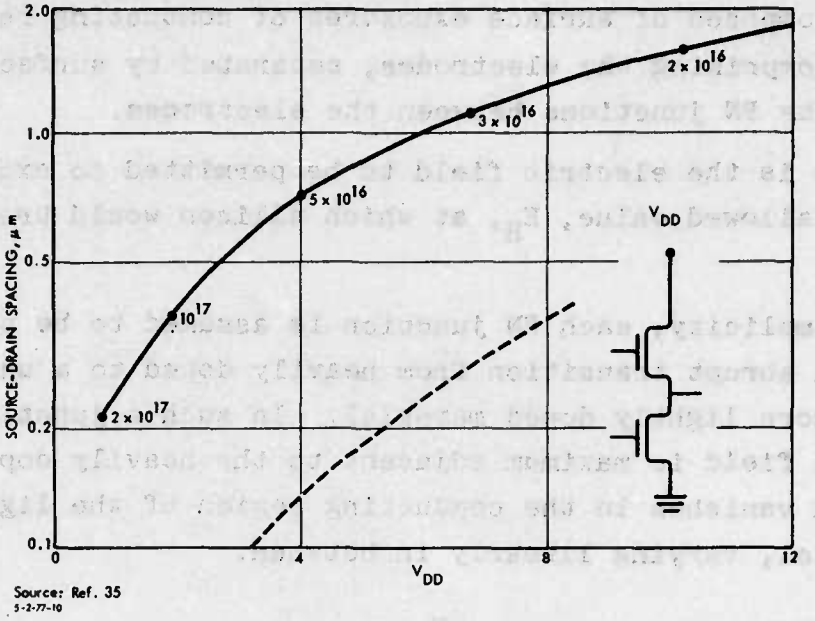

FIGURE D-1b. Physical Limits in Digital Electronics. Minimum channel length of metal-SiO_2-Silicon transistor determined by high-field breakdown of the oxide in circuit shown in insert [after Hoeneisen and Mead (43)]

elementary transistors comprise one gate, and that gates cover 40 percent of the chip surface, the remainder being needed for interconnecting leads and contacts.

1. Bipolar Transistors

The electrodes of a bipolar transistor are isolated from each other and from the substrate by PN junctions. These junctions cannot be reduced in thickness without limit because the electric fields in them would exceed the avalanche breakdown limit if the thickness were reduced too much. The potential difference across a PN junction is the sum of the externally applied voltage and the internal electron chemical potential difference between N- and P-type silicon. A collector junction is usually operated with an applied potential which adds to the internal potential difference, while an emitter has an applied potential opposite to, although usually less than, the internal potential difference.

The area of a planar bipolar transistor on the silicon surface is composed of surface exposures of conducting regions of silicon comprising the electrodes, separated by surface exposures of the PN junctions between the electrodes.

Nowhere is the electric field to be permitted to exceed the maximum allowed value, E_B, at which silicon would break down.

For simplicity, each PN junction is assumed to be planar and to be an abrupt transition from heavily doped to a uniform density of more lightly doped material. In such a junction, the electric field is maximum adjacent to the heavily doped material and vanishes in the conducting region of the lightly doped material, varying linearly in between.

$$E = \frac{N}{\epsilon} \chi ,$$

where N is the doping ion density, ϵ is the dielectric constant, χ is the distance from the edge of the conducting region of the lightly doped material, and E is the electric field strength at the point χ.

The potential difference between the conducting region of the lightly doped material and the point χ in the junction is the interval of E,

$$V = - \frac{1}{2} \frac{N}{\epsilon} \chi^2 .$$

The ratio of V to E at the surface of the heavily doped region where E is greatest is

$$\frac{-V}{E} = \frac{\chi}{2} .$$

If E is the maximum field allowable, and V is the sum of chemical potential difference and applied voltage, then the junction thickness is, disregarding the sign of V,

$$x = w = 2\frac{V}{E_B} .$$

For a junction with no applied voltage, $V = V_G = 1.1$ volts, approximately. Combining the expressions for E_B and w given above, it is possible to find the maximum allowable total potential difference across a silicon PN junction vs. the impurity atom density in the more lightly doped portion. The result is

$$V_{max} = 9.8 \times 10^7 \times N^{-0.4} .$$

Similarly, the depletion zone width, w, with this total potential difference is

$$w_{max} = 3.5 \times 10^7 \times N^{-0.7} .$$

The externally applied collector potential of a bipolar transistor must not exceed $V_{max} - V_G$, and the peak operating voltage must be less than this to provide a safety factor.

By very careful design, operating voltages of the order of one volt peak are feasible; with a safety factor of three, V_{max} could have a value of $3 + 1.1 = 4.1$ volts. The impurity density, N, corresponding to this value of V_{max}, is 2.8×10^{18} atoms/cm^3. For this impurity density, the maximum depletion width, w, would be

$$w_{max} = 3.5 \times 10^7 \times (2.8 \times 10^{18})^{-0.7}$$

$$= 4.28 \times 10^{-6} \text{ cm}$$

$$= 0.0428 \ \mu\text{m}.$$

This result, in close agreement with the data of Hoeneisen and Mead for external voltage of three volts, is approximately

the smallest depletion zone width feasible for the collector junction of a bipolar transistor.

The emitter junction typically operates at less voltage, but cannot be allowed to break down at zero voltage; a similar calculation shows that the emitter depletion width would be approximately 0.022 μm.

It is obvious that at least six PN junctions are encountered crossing a bipolar transistor along the silicon surface, so that the junctions alone, exclusive of electrode area, would make up 0.216 μm of the device diameter. The electrodes must have adequate thickness to act as conducting equipotentials at the maximum operating currents of the device, so that it is probable that the electrode thickness must be at least 0.05 μ each as exposed at the surface, except that the emitter might be slightly smaller, of the order of 0.05 μ in diameter. Then the electrode surface exposure, exclusive of junctions, would be approximately 0.25 μm. As a result, a circular planar bipolar transistor can be estimated to occupy approximately 0.216 + 0.25 = 0.466 μm in diameter, or an area of about 1/5 of 1 μm^2.

No isolation margins or safety factors have been allowed in the foregoing, so that this area is impractical by at least a factor of four.

The conclusion is that a planar bipolar transistor is estimated to have a limit to miniaturization at an area of about 1 μ^2/transistor. (Note that these dimensions are beyond the capability of optical lithography.)

A gate occupies a larger area than a single transistor since it is more complex and requires allowance for interconnections and electrode contacts. The ratio of gate area to elementary transistor area varies with the type of logic; a typical value is five (for TTL). Then the area/gate would be of the order of 5 μm^2/gate for this type of logic.

Another factor affecting density is the necessity to allow for interconnections, test pads and devices other than transistors. Present-day microprocessors have only 40 percent of their chip area actually allocated to gates, so that the effective chip area/gate would be 12.5 μm^2/gate, with similar proportions.

Gate density then would be estimated not to exceed 80,000 gates/mm^2; for gates comprised of bipolar transistors of minimum size, 5/gate.

Logic families such as I^2L might achieve higher density than this since gates can be made from fewer elementary transistors in such families.

2. Field-Effect Transistors

Breakdown of the oxide insulation between the gate electrode and the semiconductor surface is one important limitation of the miniaturization of MOS devices. In order to produce a conducting channel near the surface of the semiconductor under the gate, the surface potential must be depressed (by the gate electrode) by more than V_G, the forbidden band gap of the bulk semiconductor expressed in volts. To effect this potential depression the electric field must be transmitted by the gate electrode through a layer of insulator, usually SiO_2. The electric field in the oxide must be greater than that in the silicon in proportion to the ratio of the dielectric constant of silicon to that of the oxide. This ratio is greater than two for SiO_2, so there is a tendency for the oxide to break down before the field in the silicon reaches its breakdown value. To prevent such breakdown, the doping level of the silicon can be reduced since, with a given surface potential, the field at the silicon surface is

$$F_o = [2(V + V_G)\, Nq/\varepsilon]^{1/2}$$

which varies as the square root of the doping density, N (Refs. 35 and 44).

The effect of reducing the doping density is to make the depletion zone thicker. Since each electrode is surrounded by a depletion zone, the spacing between electrodes must be sufficient so that the two depletion zones do not overlap to an undesirable extent. From the work of Hoeneisen and Mead (Ref. 43), the minimum source-drain electrode spacing is about 1/2 μ for 3 volts between drain and substrate. Minimum area for such a device, taking into account the other geometrical constraints and requirements of an MOS transistor, is about 3/2 μ^2, not including any margin around the electrodes. Actually, the electrodes are surrounded by depletion zones, typically 1/2 μ thick, and allowing a small additional margin for isolation, the minimum area/transistor comes out to be about 6.25 μ^2. Allowing five transistors/gate, the gate area is then 32 μ^2, corresponding to 31,250 gates/mm^2. Assuming that the active area is 40 percent of the total area of the chip, there would result 12,500 gates/mm^2.

CMOS, on the same basis, would appear to provide about half as many gates/mm^2.

3. Scaling

Miniaturization of the gate structures of LSIC confers advantages other than a high level of integration: Speed of logic operations can be increased somewhat without increasing power dissipation/chip. This result is extremely important for DoD applications where speed, rather than the level of integration, is frequently a factor limiting acceptability of LSICs.

The foregoing discussion shows that miniaturization can be carried further than present practice by at least one

order of magnitude without encountering any fundamental limit. The following information shows the reasoning behind the speed improvement to be effected, following an exposition by Noyce (Ref. 6).

Assume that a logic gate of an LSIC is reduced in linear dimensions by a factor $\frac{1}{X}$, subject to the condition that all electric fields in the device shall remain constant. The constant field constraint is desirable since the present fields cannot be increased much without avalanche breakdown in either the junctions or the insulation of LSIC transistors.

The thickness of the NP junctions of the device must scale as X, therefore, to avoid increasing E, the total voltage, V, across the junction (internal plus supply voltage) must vary directly with X:

$$V \sim X.$$

For reduced junction thickness proportional to X at constant maximum field, the impurity concentrations, N, throughout the device must vary inversely with X:

$$N \sim \frac{1}{X} .$$

Current density, J, varies directly with the product of field (constant with X) and impurity concentration:

$$J \sim \frac{1}{X} .$$

Total current/transistor electrode varies as the area of the electrode times the current density:

$$I = JA \sim \frac{1}{X} \cdot X^2 \sim X .$$

Power dissipation/device varies directly as the product of V and I:

$$\dot{W} = VI \sim X^2 .$$

Number of devices/unit area varies as $\frac{1}{X^2}$, so that power dissipation/unit area is constant! Therefore, <u>miniaturization need not increase the power dissipation of a chip even though the number of devices/chip varies as the inverse square of the linear dimensions of the devices</u>.

The capacitances of the electrodes all vary directly with X; the time to change the potential by an amount, V, is

$$\tau = \frac{CV}{I} \sim X .$$

The important result is that miniaturization by scaling increases circuit speed inversely with the linear dimensions. The practical implication is that improvements in photolithography, or the use of electron beam lithography, can improve the speed of existing LSICs, provided the scaling conditions can be achieved in practice.

This is not always easy. For example, scaling requires that the potential difference between collector and base of a transistor be scaled directly with the linear dimensions. Part of this potential difference is internal to the NP junction and is due to the electron chemical potential difference between the N and P type semiconductor comprising the collector and the base; the other part is the externally applied voltage. Suppose that the externally applied voltage before change of scale is V_1, and after miniaturization by a factor $\frac{1}{X}$ the external voltage is V_2. Then, since the internal NP junction voltagt is fixed, = V_o, after change of scale the applied voltage must be considerably reduced as shown below:

$$V_2 + V_o = \frac{1}{X}(V_1 + V_o)$$

$$V_2 = \frac{V_1 - (X - 1)V_2}{X} \quad .$$

For example, if V_1 = 3.1 volts, V_o is 1.1 volts and X = 2, V_2 comes out to be 1 volt for a two-to-one reduction in size of the device. Obviously, logic families such as I^2L, which already operate on very low supply voltages (1.5 volts for I^2L), cannot be simply scaled as outlined above.

To avoid electrical erosion of metallization connecting leads, it is desirable to maintain constant thickness while scaling width of such conductors directly with X. The result is constant current density in the conductor's cross-section.

Resistors must be scaled taking into account the collector external potential anomaly noted above.

A frequently neglected fact is that heat is absorbed at a bipolar transistor emitter, nullifying the portion of collector heat output due to to the internal collector potential, V_o. Therefore, power dissipation/chip tends to be reduced, rather than remain constant with scale, if scaling is carried out in accordance with the rules set forth above.

4. Conclusions Concerning Prospects of Further Miniaturization for LSI

- The minimum area for a single planar bipolar transistor is approximately 1 μ^2.
- Assuming 40 percent utilization of the active area of a silicon chip by gates, and assuming an average of five bipolar transistors/gate, 1 mm^2 of chip could accommodate not more than 80,000 gates.
- The minimum area for a planar field-effect transistor with SiO_2 gate insulation is approximately 6.25 μ^2.

- Assuming 40 percent utilization of the active area of a silicon chip by gates, and assuming an average of five bipolar transistors/gate, 1 mm^2 of chip surface could accommodate not more than about 12,500 MOS gates.
- CMOS can provide not more than about 6250 gates/mm^2.
- The foregoing densities are approximately a factor of two orders of magnitude greater than currently available devices provide. For fundamental reasons, it is doubtful if higher densities can be achieved using planar structures on a silicon substrate.
- Scaling laws presented in Section 3, above, show how LSICs can be miniaturized to provide important benefits if photo-or electron-lithographic techniques can be further developed. Logic speed varies inversely as the first power of linear dimensions; the number of devices/chip varies inversely as the square of the linear dimensions, keeping the chip size constant; and power dissipation remains constant or diminishes as linear dimensions are reduced.

APPENDIX E

BIPOLAR DOMINANCE OF THE MSI MARKET

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Even though bipolar circuits are more expensive to produce than the MOSFETs, no MOS ICs are currently being produced in the MSI levels of integration to compete with the 54/74 series. This may seem strange considering the fact that the sales of the 54/74 series exceed the total sales of all other ICs. Of course, if MOS equivalents of the 54/74 series were offered, they could only capture the market for lower speed applications (3 mc clock speed, or lower).

This can be explained in terms of a simple supply-demand model (Fig. E-1). The upper heavy line represents the cost vs. production rate of the faster but more expensive bipolar circuits, while the lower heavy line represents the equivalent MOS circuits. Similarly, the demand curve for the faster circuits is represented by the dashed line to the upper left; the demand curve for the slower circuits is represented by the middle dashed lines, while the broken line to the right represents the total demand for both types. The total demand curve intersects bipolar productions at a lower price P_T than P_S, where the demand for slower circuits and production curves for the MOS circuits intersect, even though the slower circuits can be produced at a lower price, and the total demand at the price P_T is predominantly for the slower application.

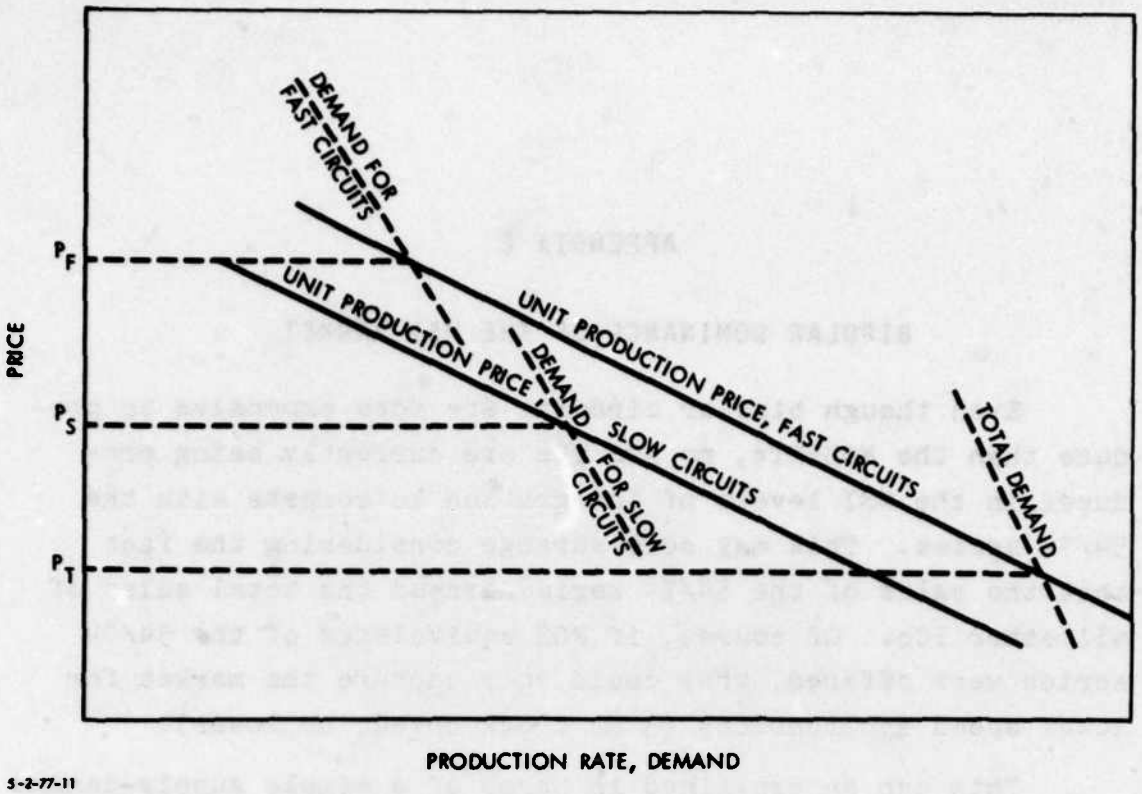
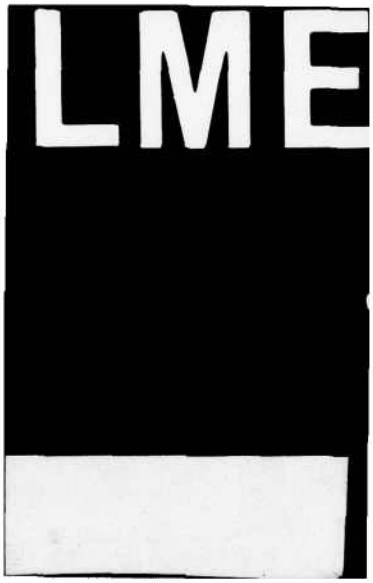


FIGURE E-1. Supply-Demand Model

In short, the faster, more expensive, circuits capture the entire market because they can satisfy both the fast and slower requirements, and this level of demand makes it possible to produce the circuits at a lower price than that of the slower circuits at the demand level of the slower applications.

For the same reason, when bipolar LSICs (such as I^2L) enter the market, they may eventually capture the entire market for circuits at their level of integration.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